

HAMILTON and AREA PACKET NETWORK.

The first meeting, an organizational and technical one, was held at the Carads Centre for Inland Waters seminar room on Sunday, January 25 at 14:00. 15 people attended and we found a lot of interest in the network among them.

This, then, is the result of that meeting: the first in a series (hopefully) of bulletins of the newly formed, nebulous group hereforth to be known as the Hamilton and Area Packet Network.

In response to requests at the meetings and our own ideas and input, this bulletin contains something for everyone.

A brief summary and minutes of the meeting is given. You will also find an introduction to SDLC Protocol from "Technical Aspects of Data Communication" by John E. McNamara. This is the protocol generated and interpreted by the Intel 8273 chip on the VANC G board.

For the person interested in entering the network, the question "What do I need to get going" is answered.

In the circuits department, you will find how I connected into the squelch circuitry of my Heath HW-202, a circuit of the modem designed by Bill Montgomery based on the Exar application note AP-01, and the circuit of my initial station node card, currently in use as a terminal node controller in my S-100 system using Modified LIP and TIP software. You will also see how to add LED indicators to the VANC G board, and some hints on setting the board running.

In the software department, Robert Sleath's TIP using the 8255 Parallel chip and interface is given. His keyboard and VRAM appear as 8-bit devices. His TIP also includes a mini monitor, entered by CTRL-B and allowing the user to load locations in RAM, dump any location in both ASCII and hex, and to jump to any location. You will also find Bill's down line loader as adapted by Stu, and a down-loadable routine to test the added LED indicators. The modification to the LIP by Stu to move RST vectors to RAM is listed, as is the portion of the LIP used to issue commands to the 8273.

Our initial mailing list is included, followed by the Exar application note and spec sheets on the 2206 and 2211.

Last, but not least is the initial Packet Radio Bibliography.

The next meeting will be called in about a month (late Feb or Mar) by phone and announcement on 146.46 and 145.65 MHz.

Things to look forward to in the next bulletin are John's (WUW) Trap dump routine and other interface schematics from Max, Glenn and John. We also hope to discuss applications.

HAMILTON and AREA PACKET NETWORK

What do I need to set going?

To begin at the beginning...

- 1) a real interest in contributing to the development of the network, either by getting involved with the implementation, or creating or making use of applications for the other users.
- 2) a 2 metre rig with either 146.46 or 145.65 (or both) cost to build - \$50 or less depending on ingenuity. (Power can be taken from VANC G PS and TTL levels can be used to connect to VANC G)
- 3) a Bell 202 modem, suitably augmented, or a simple 202 compatible one, such as that in the circuits department. Set up to run at 1200 baud using 1200 Hz and 2200 Hz tones.
- 4) a VANC G card (\$32) plus parts. VANC G no longer puts kits together, so chips might run \$250 or more. There are some SDLC chips available for about \$45 (Cdn) see Stu.
- 5) a power supply to run the VANC G board and modem. About \$40 or less (depending, again, on ingenuity)
- 6) a terminal type device! teletype, glass or otherwise, or some form of computer to emulate one. (information is available on CP/M programs for terminal emulation. APPLE and TRS-80 have similar routines, I am sure.
- 7) custom programming for your TIP. People are available who can burn 2708 EPROMs for you.

And that's about it. Except for an amateur license of course (wish me luck with the code!!!).

A digital license is not required since the mode in use is F2 (AFSK), and when we move to 220, just plain FSK.

MAKE GOOD THINGS HAPPEN.

2391 Arnold Crescent,
Burlington, Ontario,
L7P 4J2, Canada.

ALL DONATIONS CHEERFULLY ACCEPTED!

CHAPTER 19

SDLC AND BIT ORIENTED PROTOCOLS

It is not the intent of this chapter to be a definitive source on SDLC, but rather to describe enough of its operation for the reader to get the general idea and to be able to more readily understand more detailed references on the subject.

First, a few definitions should be given. Any data communication link involves at least two participating stations. The station which has responsibility for the data link and which issues the commands to control that link is called the "primary station." The other station is a "secondary station." It is not necessary that all information transfers be initiated by a primary station. Using SDLC procedures, a secondary station may be the initiator.

The basic format for SDLC is a "frame," shown in Figure 19-1. The information field is not restricted in format or content and can be of

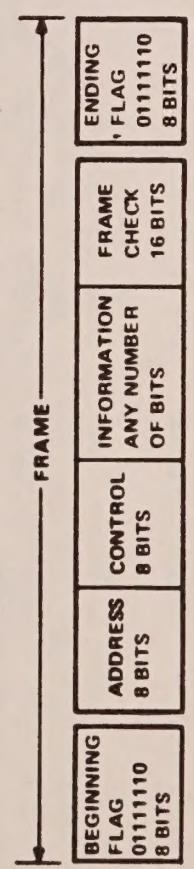


Figure 19-1. Basic SDLC Frame

any reasonable length (including zero). The maximum length is that which can be expected to arrive at the receiver error-free most of the time, and is hence a function of communication channel error rate.

The two flags which delineate the SDLC frame serve as reference points for the position of the address and control fields and initiate the transmission error checking. The ending flag indicates to the receiving station that the 16 bits just received constitute the Frame Check. The ending frame could be followed by another frame, another flag, or an idle. Note that this means that when two frames follow each other, the intervening flag is simultaneously the ending flag of the first frame and the beginning flag of the next frame. Since the SDLC protocol does not use characters of defined length, but rather works on a bit by bit basis, the 0111110 flag may be recognized at any time.

In order that the flag not be sent accidentally, SDLC procedures require that a binary 0 be inserted by the transmitter after any succession of five continuous 1s. The receiver then removes a 0 that follows a received succession of five 1s. Inserted and removed zeros are not included in the transmission error check.

The address field is eight bits long and designates the number of the secondary station to which the command from the primary station is being sent. The control field is an additional eight bits and can have three formats: "information transfer format," "supervisory format," and "nonsequenced format." The only thing in common between the three formats is the P/F (poll/final) bit. A frame with the P(poll) bit set is sent from a primary station to a secondary station to authorize transmission, and a frame with the F(final) bit set is sent by the secondary station in response to the poll. Typically, the primary station will send a number of frames to a particular secondary station, each frame having the P/F bit a 0, until the primary station is finished and ready for the secondary station to respond. At this time the primary station will send a frame having the P/F bit set to 1. The secondary station will recognize that the primary station desires a response and will reply, perhaps with a number of frames, each having the P/F bit a 0. Then, when the secondary station is completing its response to the "poll," it will send a "final" frame which has the P/F bit set to 1.

The three control formats are summarized in Table 19-1.

Table 19-1. SDLC Control Field Formats

Format	Bits	Acronym
Information	Nr P/F	Ns 0 I
Supervisory	Nr P/F	00 01 RR
	Nr P/F	01 01 RNR
	Nr P/F	10 01 REJ
Nonsequenced	000 P/F	00 11 NSI
	000 F	01 11 ROI
	000 P	01 11 SIM
	100 P	00 11 SNRM
	000 F	11 11 ROL
	010 P	00 11 DISC
	011 F	00 11 NSA
	100 F	01 11 CMDR
	001 F	00 11 ORP

Sent First →

Sent Last →

The supervisory format is used in conjunction with the information format to initiate and control information transfer in the information format. The first two bits sent, 1 and 0, designate that this control field is in supervisory format. The next two bits indicate which command this is: RR, RNR, or REJ. An RR (Receive Ready) can be sent by either a primary or a secondary station, and indicates that all sequenced frames up through Nr-1 have been received correctly, and that the originating station is ready to receive some more. RNR (Receive Not Ready) can also be sent by either a primary or a secondary station, and also acknowledges messages up to Nr-1. Unlike RR, however, RNR indicates a temporary busy condition in which no additional frames that require buffer space can be accepted. REJ (Reject) is a command/response which may be transmitted to request transmission or retransmission. It acknowledges successful receipt of frames up through Nr-1 and requests Nr and following frames.

The nonsequenced format is used for setting operating modes, initializing stations, etc. As the name implies, nonsequenced communications are not sequence checked and do not use the Nr and Ns system. The first two bits sent, 11, indicate a nonsequenced format, the P/F bit has its usual meaning, and the remaining five bits in the control field are used for encoding the various commands and responses.

The commands and responses encoded in the nonsequenced format control field are listed below.

NSI (Nonsequenced Information): This indicates that the information which follows in the variable length information field is being sent separately from any sequenced message presently in progress.

RQI (Request for Initialization): This is transmitted by a secondary station when it wishes the primary station to send an SIM command. If the primary station sends something other than SIM, the secondary station sends another RQI.

SIM (Set Initialization Mode): This command initiates system-specified procedures at the receiving secondary station for the purposes of initializing. Nr and Ns counts are set to 0 at both the primary and secondary stations. The expected response to SIM is NSA.

The information format is used for ordinary data transmission and is the only one of the three formats that uses frame sequence numbering. Each frame transmitted in this format is numbered so that the receiving station can tell if any are missing; when retransmission is required, the receiving station can tell the transmitting station which frame to start with in the retransmission. A station that transmits sequenced frames counts and numbers each frame. This count is known as Ns. A station receiving sequenced frames counts each error-free sequenced frame that it receives; the receiver count is called Nr. The Nr count advances when a frame is checked and found to be error-free; Nr thus becomes the count of the "next expected" frame and should agree with the next incoming Ns count. Returning to the format shown in Table 19-1, the initial 0 bit indicates that this control field is in information format, the three Ns bits are "this is the message number I am sending," the P/F bit is set if the station is concluding its poll or its response to a poll, and the three Nr bits are "this is the message number I am expecting next."

SNRM (Set Normal Response Mode): This command subordinates the receiving secondary station to the transmitting primary station, and the secondary station is not expected to initiate any transmissions unless requested to do so by the primary station. The Nr and Ns counts at both the primary and the secondary stations are reset to 0. The secondary station remains in this mode until it receives a DISC or SIM. The expected response to SNRM is NSA.

ROL (Request On-Line): This is transmitted by a secondary station to indicate that it is disconnected.

DISC (Disconnect): This command places the secondary station effectively offline. That station cannot receive or transmit information frames and remains disconnected until it receives an SNRM or SIM command. The expected response to DISC is NSSA.

NSA (Nonsequenced Acknowledgement): This is the affirmative response to SNRM, DISC, or SIM.

CMDR (Command Reject): This is the response transmitted by a secondary station in normal response mode when it receives a non-valid command. A frame with CMDR in the control field has an information field following which is arranged in a fixed format which reports that station's present Ns, that station's present Nr, and four bits which indicate 1) an invalid or non-implemented command, 2) an information field associated with a command which isn't supposed to have one, 3) an information field that was so long it caused buffer overrun, or 4) the Nr received from the primary station does not make sense, given the Ns that was sent to it.

ORP (Optional Response Poll): This command invites transmission from the addressed secondary stations.

While SDLC is simpler in most aspects than previously discussed protocols, the block check calculations are a good deal more complex. The first difference is that the transmitting station begins with a "remainder value" of all 1s rather than the customary all 0s. The binary value of the transmission is premultiplied by X^{16} and divided by the generating polynomial $X^{16} + X^{12} + X^5 + 1$. The quotient digits are

ignored and the transmitter sends the complement of the resulting remainder value, with the high order bit first.

One other feature which should be discussed is the procedure for prematurely terminating a data link. This is called "abort" and is accomplished by the transmitting station's sending eight consecutive 1 bits. The abort pattern may be followed by a minimum of seven additional 1s to idle the data link, or it may be followed by a flag. The purpose of a flag following an abort is to clear the CRC function at the receiver.

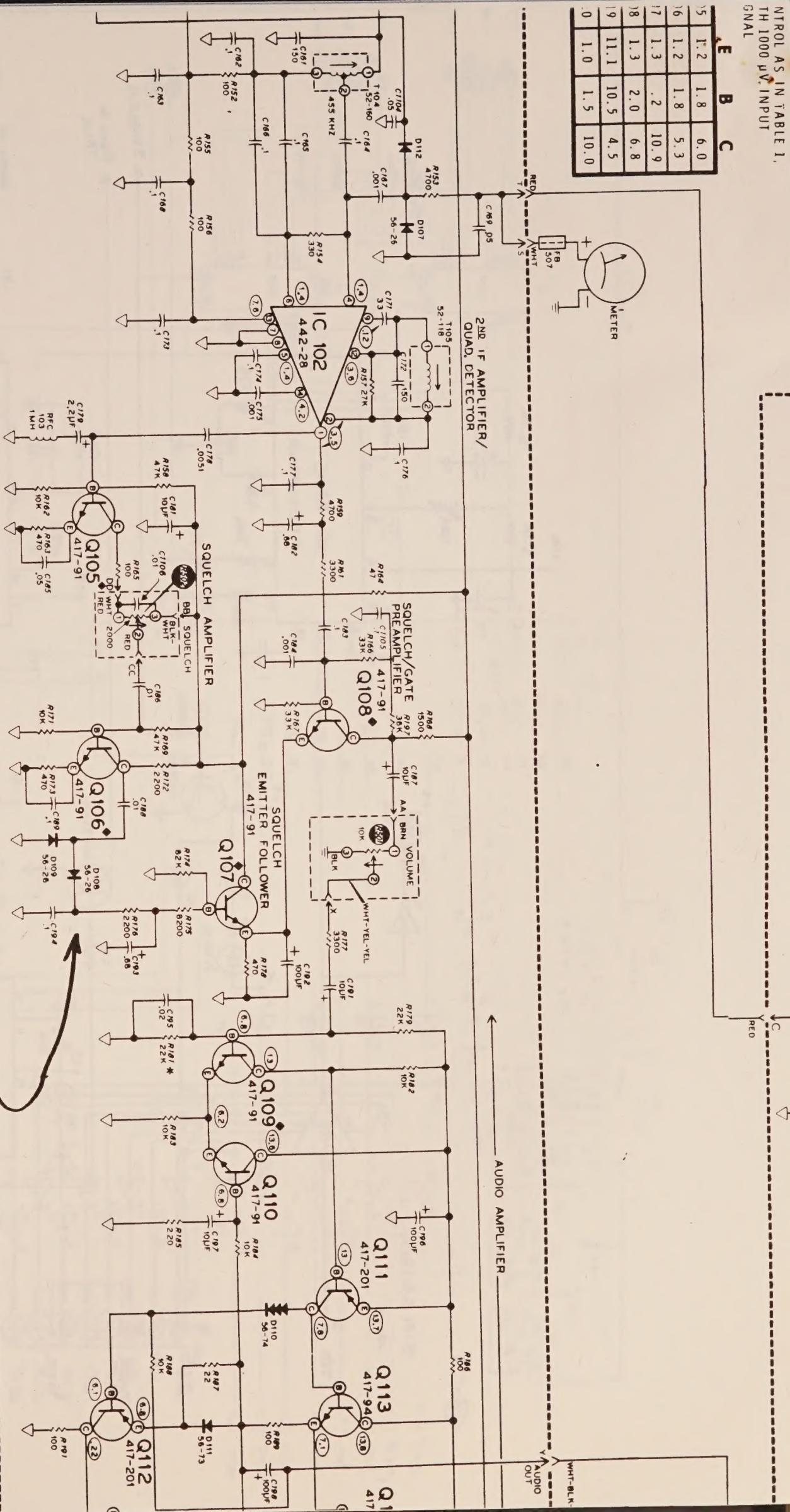
The preceding has been a rather condensed description of SDLC and the reader is advised to read IBM's "IBM Synchronous Data Link Control — General Information" (GA27-3093 File GENL-09) for further information. The reader is also referred to documentation on ADCCP and HDLC for a look at some similar protocols.

**DONATIONS TO HELP WITH
PUBLICATION COSTS AND
POSTAGE CHEERFULLY
ACCEPTED**

Comments:-

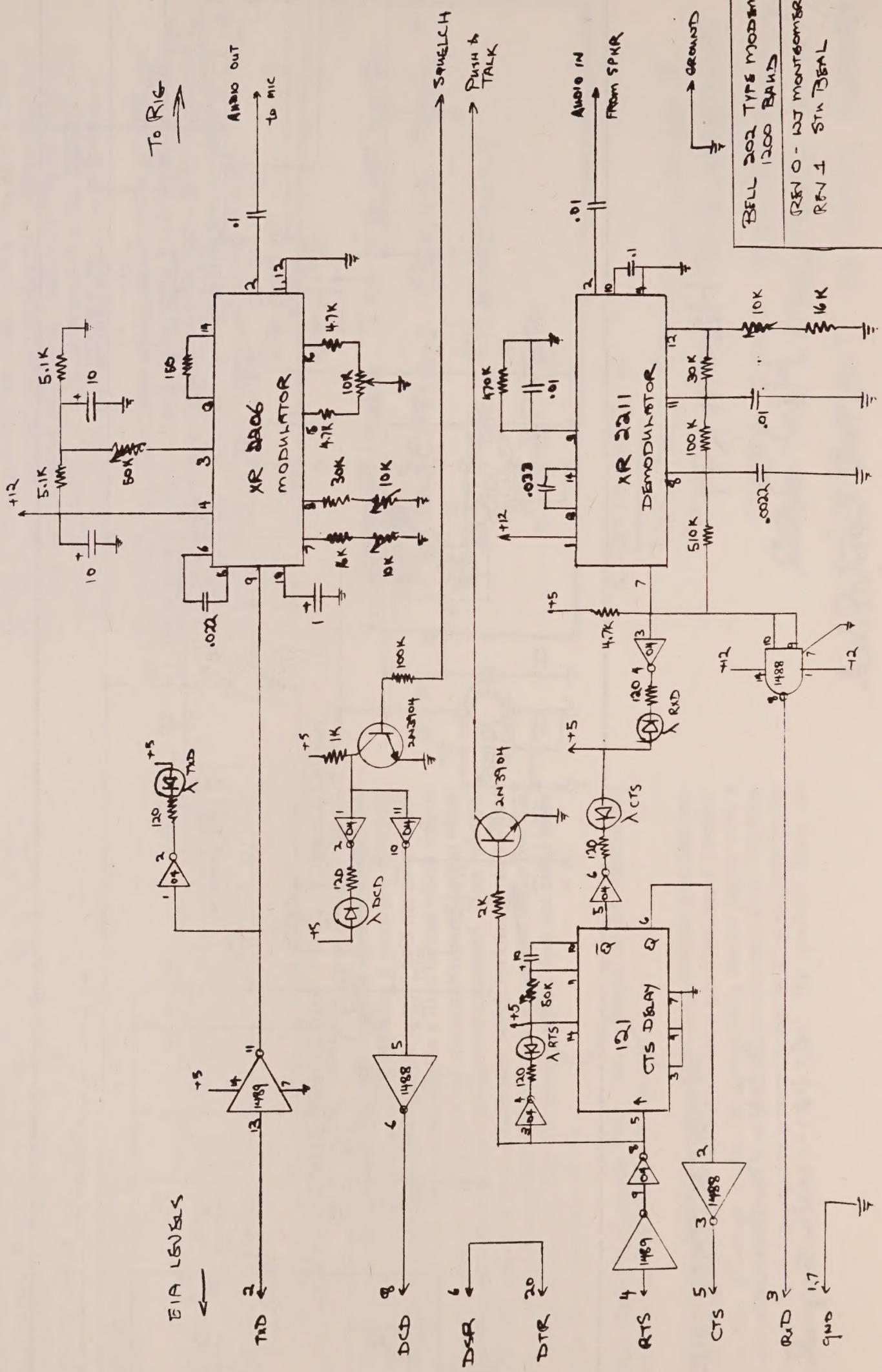
**DIGITAL COMMUNICATION &
MODULATION BIOGRAPHY**
MORE THAN 200 REFERENCES
FROM THESE LITERATURES AND
GOVERNMENT CONTRACT REPORTS.

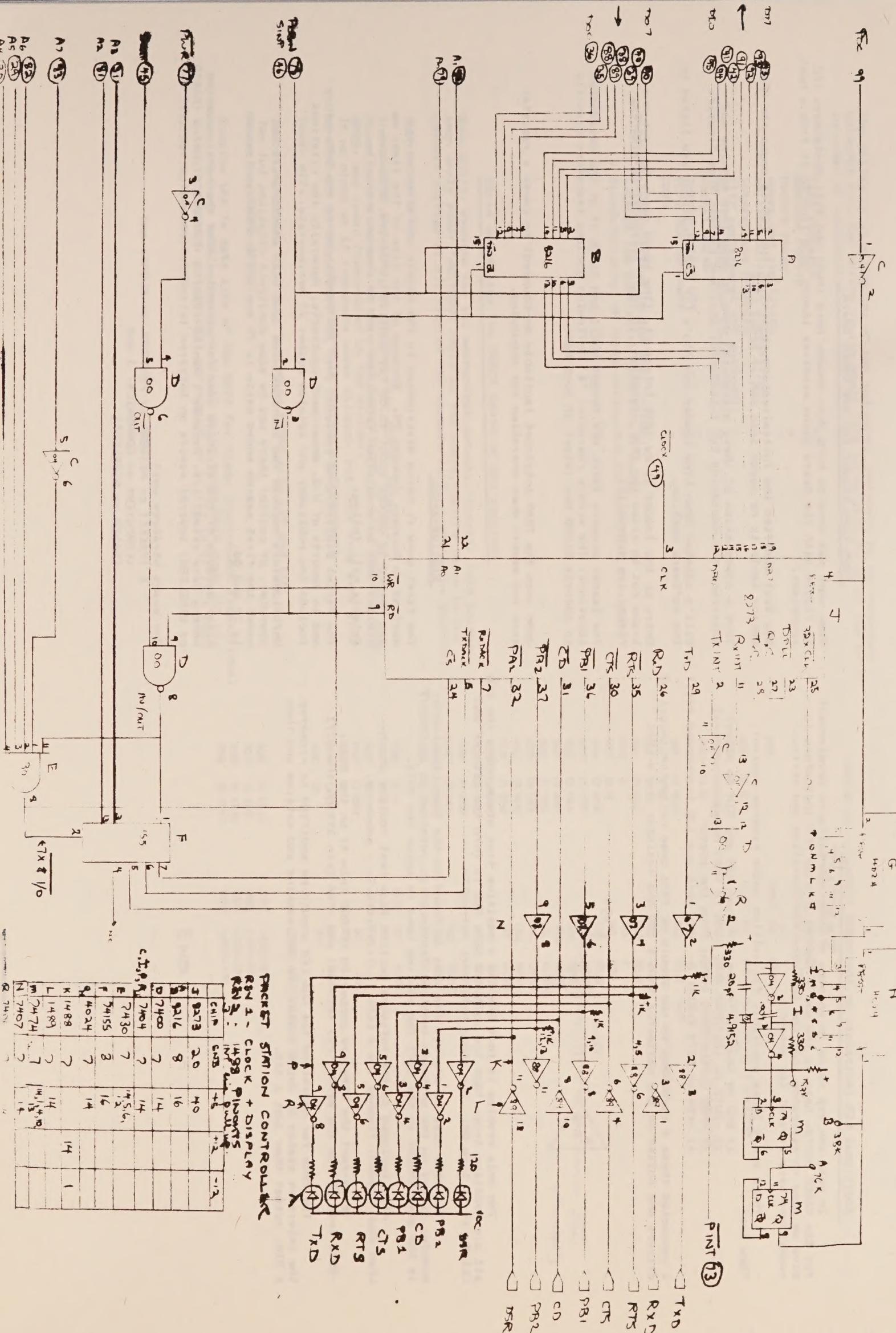
NTROL AS IN TABLE 1, TH 1000 μ V INPUT GNAL			
15	1.2	1.8	6.0
16	1.3	.2	10.9
17	1.3	2.0	6.8
18	1.3	2.0	4.5
19	11.1	10.5	10.0
20	1.0	1.5	10.0



SQUELCH TAKE OFF
 ≈ 5 V no carrier
 < 1 V with signal

HEATH KIT
HW 202
 Xtal controlled.





Additional LED indicators on the VANC6 board.

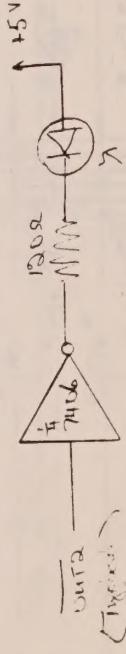
In case you are going to do some of your own software development for the VANC6 board, here is the way I hooked up some LED indicators to give me some re-assurance that the software was operating and certain conditions were present (or absent).

There are 4 lines available for setting under program control.

They are:

- 1) SOD on the 8085 processor (use RIM and SIM to alter)
- 2) -OUT2 on the 8250 UART (I/O to UART command register)
- 3) -PB3 on the 8273 (point F on the board)
- 4) -PB4 on 8273 (point G- for both use I/O to command reg.)

I connected these 4 locations to the inputs of 7406 open collector inverters, drivers and pulled up the collector thru a 120 ohm resistor and a LED:



The only problem is that SOD has a positive true state while the other three are negative true. Thus the software SETS SOD to turn the LED OFF and CLEARS it to turn ON. The other bits work correctly.

The code used to operate the LEDs is found in the Down Line Loader module, listed in the software section. The location referred to as CMDOUT is the same CMDOUT in the LIP; the routine used to setup the 8273.

Also included in the software section is a test routine which, when down loaded, flashes the 4 LEDs in 1,2,3,4,i,2,... sequence,

To re-cap: the LEDs are connected to SOD (Pin 4) on the 8085, -OUT2 (Pin 31) on the 8250, -PB3 (Pin 38) and -PB4 (Pin 39) on the 8273.

The code for operating the SOD LED should be modified to preserve the interrupt states by doing a RIM, the SOD masking and setting and then a SIM, rather than just a SIM.

Down Line Loader for the VANC6 board.

Some work was done by both John, Vanden Berg (NUU) and Bill Montomery (EC) to fiddle with the board using programs loaded down line to it from a host processor.

Stu Real modified the initialization portion of the LIP to cause the RST vector table to be moved into RAM at RESET time.

Thus a combination of these allows the user to down load modules and intercept the vectoring for interrupts, etc. and process them himself.

Bill's adarted Down Line Loader and Stu's LIP modifications are listed in the software section.

Entry to the loader is by TRAP interrupt. (The board needs to have one trace cut to allow the TRAP operation. It isn't difficult to find the place: see schematic)

The loader accepts INTEL HEX format ASCII and loads it at the designated locations. The single character '*' following loading transfers directly to address 0100 Hex (start of real RAM).

John uses the TRAP interrupt (suitably de-bounced) to cause a register save and memory dump operation for debugging.

The first copy is being distributed to the people who attended the meeting on Sunday, January 25. Because of the size of the item, we are forced to charge about \$5.00 for additional copies. A second bibliography on modulation techniques will be available shortly. Details will follow.

The Packet bibliography contains over 200 references to the literature and to reports of U.S. government contracts. Generally the citations include the publisher and catalog number if appropriate. Unfortunately because two searches were done some months apart (by computer, of course) there may be some duplicate citations but, not many; the first search ended early in 79 and the second was limited to 79 and 80.

Also, because of the strategy used for searching some (perhaps) unwanted papers were cited: i.e. because I wanted (DIGITAL COMMUNICATION) & (RADIO (COMPUTER*) OR COMMUNIC*)] and (RADIO OR WIRELESS)

The exact strategy was:
[(PACKET OR NETWORK OR PROTOCOL OR ALOHA) and
(COMPUTER* OR COMMUNIC*)] and
(RADIO OR WIRELESS)

The following is a summary of the indicated interests in the proposed network; i.e., the things people would like to be able to do on the net. In order of popularity:

file transfer	12
message centre	10
packet video	9
games and simulation	7
on line bulletin composition	7
interactive graphics	7
RTTY replacement (HF gateway)	6
on-line swap shop classifiers	6
packet voice	6
remote system use	5
VET, VE2 gateways	5
CBBS	4

Other interests listed in the Etc. column:

Promote low cost entry into Packet Radio Standardization	on State-of-the-Art Hardware and Protocols
--	--

Hints on setting the VANC6 board up and running.

Once built, examine for all mechanical defects (shorts, cold solder) then apply power WITHOUT chips on the board. Verify there is the correct voltage at all pins of the sockets (+5, +12, open, ground).

Turn power OFF!

Insert 8085 and XTAL and divider chip (CMOS... careful). Power up and attempt to see clock transitions at 1/2 clock out from 8085, and lower frequencies on the divider. If no clock or if frequency seems strange, put 20PF from each side of XTAL to ground. (Seems to help startup on-frequency.)

Power off.

Insert remainder of chips, including ROMS with LIP and TIF.

Power on (SMOKE TEST).

Examine the Tx data line of the 8273 for flags (continuous transitions). The DTR line (-PB2) should go to -12 while reset held down (+4 if only TTL outputs, not RS-232) and should go to +12 (0 if TTL) soon after button released.

DLTEST

```

; INCLUDE REGS.REF
; 9250 SERIAL ;0 ENATES
; ,LISI
; CMOUT E00 0AE8H
; FLASH: MUL A,040H ;MAKE SOUT LOW TO TURN LED ON
; SIM ;TURN IT ON
; CALL DELAY ;WAIT A BIT
; ORI 080H ;RAISE SOUT LINE TO TURN LED OFF
; SIM ;DO IT
; CALL DELAY ;WAIT
; OUT MUL A,0402 ;GET BIT FOR OUT2 LED
; OUT MCR
; CALL XRA AF
; OUT MCR
; CALL DELAY
; LXT H,CMD3
; CALL CMOUT
; CALL DELAY
; LXT H,CMD4
; CALL CMOUT
; CALL DELAY
; LXT H,CMD1
; CALL CMOUT
; CALL DELAY
; LXT H,CMD2
; CALL CMOUT
; CALL DELAY
; JMP FLASH
; DELAY: MUL H,100
; ,L03: MUL L,0
; ,L04: DCR L
; JNZ ,L04
; DCR H
; JNZ ,L03
; RET
;
; COMMAND FOR LINES ON AND OFF
; C001: 1,063H,010H
; C002: 1,063H,0F0H
; C003: 1,063H,00H
; C004: 1,063H,0F0H
;
```

END

TIP B₂

R. SLEATH (V83SFND)

CF/M MACRO ASSEM 2.0 #001 VADIC TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-B

CF/M MACRO ASSEM 2.0 #002 VADIC TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-TT

```

TITLE 'VADIC TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-B'
; VADIC TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-TT
; VADIC TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-B
; BY DOUG LOCHHAAS, VETUSI
; MAI-1980
; LAST CHANGER: BY R.SLEATH
; 20 NOV 90
; TERMINAL INTERFACE PROGRAM
; THIS PROGRAM IS WRITTEN TO RUN IN THE VADIC TERMINAL MODE CONTROLLER.
; IT INTERFACES WITH A NODE COMMUNICATIONS PROGRAM RUNNING AT ADDRESS 0 IN
; MEMORY. THIS VERSION IS WRITTEN TO USE THE 8085 PROGRAMMABLE I/O PORT
; TO COMMUNICATE WITH A LOCAL TERMINAL.

```

MACLIB LIB85

```

INCRTB MACRO
    MVI    A+1
    RST    2
    ENDM
INCRLB MACRO
    MVI   A+?0
    RST    3
    ENDM

```

```

; RAM CONSTANT - CHANGE FOR DIFFERENT RAM LOCATION
LDRAM EQU 1000H ; START OF RAM STORAGE

```

```

; NON-ZERO STATUS MEANS LINE BUFFER ADDRESS IS IN HL REG,
; ZERO STATUS MEANS NO BUFFER IS READY
NEXTIN MACRO
    RST    4
    ENDM

```

; 8255 PARALLEL I/O EQUATES

```

0008 = PORTA EQU 8      ; PORT A INPUT AND OUTPUT
0009 = PORTB EQU 9      ; PORT B INPUT AND OUTPUT
000A = PORTC EQU 0AH     ; PORT C INPUT AND OUTPUT
000B = CONTROL EQU 0BH    ; CONTROL PORT OUTPUT ONLY

```

0017 = RIMD EQU 17H ; REQUEST INITIALIZATION MODE CONTROL BYTE

0008 = MSE EQU 08H ; MASK SET ENABLE BIT

PAGE

; COMMON COMMUNICATIONS AREA

; CIRCULAR TERMINAL BUFFER VARIABLES

```

        LDRAH EQU 1000 ; ADDRESS OF BEGINNING OF COMMON COMMUNICATIONS AREA
        CCR4A EQU 0004 ; CURRENT TERMINAL BUFFER INPUT ENTRY
        CCA4A EQU 0005 ; OLDEST TERMINAL BUFFER ENTRY
        CCAB8 EQU 0006 ; TERMINAL BUFFER INPUT POINTER
        CCA0AH EQU 0007 ; TERMINAL BUFFER OUTPUT POINTER
        CCA10H EQU 0008 ; LAST TERMINAL BUFFER OUTPUT ENTRY
        CCA10H EQU 0009 ; CURRENT TERMINAL BUFFER OUTPUT ENTRY

```

; CIRCULAR LINE BUFFER VARIABLES

```

        LBPE EQU 1012 ; LINE BUFFER PROCESSING ENTRY
        CLBE EQU 0004 ; CURRENT LINE BUFFER ENTRY ADDRESS
        OLBPE EQU 0016 ; OLDEST LINE BUFFER ENTRY
        LRIP EQU 0018 ; LINE BUFFER INPUT POINTER
        LR0F EQU 001A ; LINE BUFFER OUTPUT POINTER

```

; MISCELLANEOUS

```

        STAT1 EQU 1000 ; MAINLINE STATUS BYTE
        TROFL0 EQU 1003 ; TERMINAL BUFFER OVERFLOW STATUS
        BUFCOUNT EQU 101C ; CURRENT INPUT BUFFER COUNT
        OUTCOUNT EQU 101D ; CURRENT OUTPUT BUFFER COUNT
        BYTES REMAINING
        CR EQU 000D ; ASCII CARRIAGE RETURN
        LF EQU 000A ; ASCII LINE FEED

```

PAGE

CP/M MACRO ASSEM 2.0 #003 VACIG TERMINAL NODE COMMUNICATIONS PROGRAM - M6

U.S. MARCH ASSETS 2.3 TRILLION DOLLARS, 2008 CHARTERED BANKS, FEDERAL RESERVE

CP/M MACRO SYSTEM 2.0 1005 VARIOUS TERMINAL MODE COMMUNICATIONS PROGRAMS - MODULE TIP-II

```
0800      ; WHERE THIS PROGRAM'S JUMP TABLE IS
```

```

083E F5      E3155; PUSH    C5H
083F E5      PUSH     H
0830 F5      PUSH     I
0831 C5      PUSH     R
0832 D80A    EXITM:  OH

```

089943E01
08994D7
089C220410
089F72A7998
09A231FF
0B01
651
657
SMB
6M2
SK1P
WU1
A+OFFH

```

; RST155 ; INTERRUPT FROM R255
; UNUSED INTERRUPT ENTRY POINT
; DISPATCH ; TO DISPATCHER ROUTINE
; 12,RIMU,'WESEF' ; CONNECTION BUFFER
; 8,RIMU ; THIS MODES TERMINAL NUMBER

TIPINIT:
    RIM ; UNMASK INTERRUPTS FROM SERIAL INTERFACE
    ; GET CURRENT INTERRUPT MASK IN A
    DB 20H ; SET MASK
    AMI 00000100 ; RESET RST15.5 MASK BIT
    ORI MSE ; SET MASK SET ENABLE BIT
    STM ; ENABLE RST15.5 INTERRUPTS
    DB 30H ; JUMP

0815120
0816 E606
0818 F608
081A130
081B 3E89
081D D20B
081F AF
0820 D30B
0822 3D
0823 030B
0825 CDF008
0828 21E909
082B C3D009

    OUT A,89H
    OUT 0BH
    A
    OUT 0BH
    A
    OUT 0BH
    CALL CLEAR
    LXT H,MESSG1
    JMP MESSOUT

; RETURN TO RDP FOR COMPLETION OF INITIALIZATION

```

```

; ECHO DATA TO TERMINAL
M
I
H
LXI H,BUFCONT
IMR
M
H
MOV H,A
ANT ZFH
IMR
TBLD TBIP
LMD LMD
XORL XORL
OTRE OTRE
JZ JZ
MINIM MINIM
TROFID TROFID
A A
EXIT EXIT
JNZ JNZ
CALL CALL
UPSCRN UPSCRN
EXIT EXIT
JMP JMP
CALL CALL
CLEAR CLEAR
INTINT INTINT
JZ JZ
CALL CALL
INTINT INTINT
OTRE OTRE
; DE <-- OTRE
TBIP TBIP
MERIT MERIT
IMR IMR
A1 A1
2 2
FULL FULL
TBLD TBLD
IMR IMR
0AH 0AH
ANT ANT
ZFH ZFH
H,A H,A
; ECHO DATA TO TERMINAL

```

08A743E01	Skip:	INORTB
08A94D7	NUT	A,1
08AA220810	RET	2
08A0C2B508	SHLD	TRIP
08B0JEFF	JNZ	EXIT
08B2320310	TR0FL	TR0FL
08B5AF	STA	A
08B6D208	OUT	0BH
08B83D	INC	A
08B9D308	OUT	0BH
08BBFB	EL	EL
08BCCUAD09	CALL	UPSCRN
08BF C1	POP	R
08C0D1	POP	D
08C1E1	POP	H
08C2F1	POP	PSM
08C3C9	RET	EXIT
0BC43EFF	FULL	A,OFFH
08C6320310	STA	TR0FL
08C9C3B508	JMP	EXIT

CP/M MACRO ASSEM 2.0

CP/M MACRO ASSEM 2.0

CP/M MACRO ASSEM 2.0

1011

VANCE TERMINAL NODE COMMUNICATIONS PROGRAM - MODULE TIP-TI

0009 VANCE TERMINAL NODE COMMUNICATIONS PROGRAM

VANCE TERMINAL NODE COMMUNICATIONS PROGRAM

VANCE TERMINAL NODE COMMUNICATIONS PROGRAM - MODULE TIP-TI

0081 J9

DAT

SF

STKTR

SHLD

LXI

H,140H

XCHG

CALL

RUMNUM2

DUMP:

CALL

RUMNUM2

DUMP:

CALL

RUMNUM2

LOAD:

CALL

RUMNUM2

; DUMP COMMAND PROCESSOR

DUMP:

CALL

RUMNUM2

DUMP:

CALL

FROM LIA

0895	3E00	0RLF:	MVI	A,0DH
0B97	C06209		CALL	CHOUT
0B9A	C3A109		JMF	UPSCRN
		;		
OPEN	DEBA	STATICS	W	CON

OB9F	E80	AM1	E0H
OB9I	C9	RET	
OB92	CD9DBB	KRDN:	CALL
OB95	5AA20B	JZ	KBDIN
OB98	AF	XRA	A
OB99	D30B	OUT	OBH
OB9B	3D	DCR	A

Issue Date
+ 8273

VADG TERMINAL NO. 111-12345678
VADG TERMINAL NO. 111-12345678

0B8A 05	PUSH B	008D	C8
0BBB C5	PUSH B	008E	23
0B8C C3D209	JMP CLEAR!	008F	05
		0090	D8 10
		0092	E6 20
		0094	C2 0090
		0097	7E
		0098	D3 11
		009A	C3 008B

MESSAGE AREA

VADCG TERMINAL NODE COMMUNICATIONS PROGRAM MACRO-90 3.35 17-Mar-80 PAGE 1-2
LIF-MAIN MODULE

VAUCL TERMINAL NODE COMMUNICATIONS PROGRAM MACRO-80 3.36 17-Mar-80 PAGE 1-3
LIF-MAIN MODULE

```
; MODE COMMUNICATION PROGRAM MAINLINE
; INTERRUPT VECTORS
; LOW ROM interrupt and RST dispatchers.

; This code appears here, before the majority of the symbols used
; are defined so that KLUSELN can be calculated before it is used
; in the parameterization of the memory allocation. This prevents
; a phase error in assemblies.

0000' CSEG
0000' ORG 0
RESET' JMP INIT ; ORIGIN AT 0, MUST RUN AT 0!
; ENTRY POINT WHEN RESET BUTTON IS PRESSED
; ENTRY POINT WHEN RESET BUTTON IS PRESSED
0008' C3 1002
; JMF RST1 ; GO TO DISPATCH IMAGE IN RAM
; JMF RST2
0010' C3 1005
; ORG 10H
; JMF RST2
0018' C3 1000
; ORG 18H
; JMF RST3
; ORG 20H
; JMF RST4
0020' C3 1015
; ORG 24H
; JMF TRAP
0024' C3 1019
; ORG 28H
; JMF RSTS
0028' C3 101C
; ORG 2EH
; JMF RST55
002C' C3 1020
; ORG 30H
; JMF RST6
0030' C3 1023
; ORG 34H
; JMF RST65
0034' C3 1026
; ORG 38H
; JMF RST7
0038' C3 1029
; ORG 3CH
; JMF RST75
003C' C3 102C
PAGE PAGSIZ
1020' C3 0000t
005F' C3 0000t
1023' C3 0000t
0062' C3 0000t
1026' C3 0000t
0065' C3 0000t
1027' C3 0000t
0068' C3 0000t
1028' C3 0000t
1029' C3 0000t
RS165 EOU
JMP TXINT
; TXINT ; 8273 TRANSMIT INTERRUPT
RST6 EOU
JMP $-RSTSTAR+ACTRAM
; -RSTSTAR+ACTRAM ; ALTMODE ; ALTERNATE MODE FROM MONITOR TO CONNECT AND WU
RST17 EOU
JMP $-RSTSTAR+ACTRAM
; -RSTSTAR+ACTRAM ; GO TO TERMINAL INTERFACE PROGRAM JUMP TABLE
RS175 EOU
$-RSTSTAR+ACTRAM
```

; THIS IS AN IMAGE OF THE DISPATCH AREA WHICH IS MOVED TO
; 0100H AT INITIALIZATION TIME SO RST TYPE DISPATCHES CAN
; TAKE PLACE NORMALLY, BUT CAN BE WRITTEN OVER BY DOWNLOADED
; PROGRAMS.

; RST1 EOU \$
; DS 2 ; SPACE FOR STACK POINTER IN MINIMONITOR
; RE-LLOCATES TO 1000H

; RST2 EOU \$-RSTSTAR+ACTRAM
; PUSH B
; PUSH D
; CALL INCRLB
; POP D
; POP B
; RET

; RST3 EOU \$-RSTSTAR+ACTRAM
; PUSH B
; PUSH D
; CALL INCRLB
; POP D
; POP B
; RET

; RST4 EOU \$-RSTSTAR+ACTRAM
; PUSH D
; JMP NXTRM2 ; GETS NEXT LINE BUFFER ENTRY FOR TIP

; TRAP EOU \$-RSTSTAR+ACTRAM
; JMP INLOAD ; DOWN LOADER ENTERED FROM 'TRAP' SWITCH

; RST5 EOU \$-RSTSTAR+ACTRAM
; PUSH B
; COMPLH ; SAVE BC ON STACK
; CMPHL ; GO TO COMPARE HL WITH DE

; RST15 EOU \$-RSTSTAR+ACTRAM
; TXINI ; GO TO TERMINAL INTERFACE PROGRAM JUMP TABLE

; RST6 EOU \$-RSTSTAR+ACTRAM

; RST17 EOU \$-RSTSTAR+ACTRAM

; RST175 EOU \$-RSTSTAR+ACTRAM

```

VADCG TERMINAL MODE COMMUNICATIONS PROGRAM          MACRO-90 3.36   17-Mar-80      PAGE  14
LTS-MAIN MODULE                                     MACRO-90 3.36   17-Mar-80      PAGE  15

006B' C3 0000#                                JMF    RXINT  ; 9273 FEEF1C INT10HIF
                                                ; RSTEND+RSTAB
006E'          ; RSTEND EQU
007F'          ; RSTLEN EQU
                                                ; MEMORY CONFIGURATION EQUATES
                                                ; LDROM depends on the length of the kluge table
102F          LORAM  EQU  ACTRAM+RSTLEN           ; FIRST BYTE OF CONTIGUOUS RAM AREA
1FFF          HIRAM  EQU  ACTRAM+OFFH            ; LAST BYTE OF CONTIGUOUS RAM AREA
                                                ; INCLUDE CCA.REF
C             COMMON COMMUNICATIONS AREA PUBLIC DECLARATIONS AND DEFINITIONS
C             .LIST
                                                ; INCLUDE STATUS.DEF
C             STATUS BIT DEFINITIONS FOR STAT1,2,3 AND CEOF
C             .LIST
                                                ; PAGE    PAGSIZ
                                                ; INITIALIZATION CODE
                                                ; ENTERED FROM RESTART INTERRUPT
                                                ; MOVE THE RST DISPATCH TABLE TO RAM
006E' F3          INIT:  BI      ; 01      ; DISABLE INTERRUPTS
                                                ; MOVE THE RST DISPATCH TABLE TO RAM
006F'          11 003F'  LXI  D,RSTTAB        ; GET ADDRESS OF SOURCE FOR MOVE
0072' 21 1000  LXI  H,RCTRAM        ; GET ADDRESS FOR DESTINATION
0075' 06 2F      RVI   R,RSTLEN        ; GET COUNT OF ITEMS TO MOVE
RSTM0V:       LDAX  D      ; FETCH A BYTE TO MOVE
                MOV   H,A  ; STORE AT DESTINATION
                INX   D      ; UPDATE SOURCE POINTER
                INX   H      ; AND DESTINATION POINTER
                DCR   B      ; COUNT OFF THE BYTE
                JNZ   RSTM0V  ; COUNT OFF THE BYTE
                                                ; SET UP STACK POINTER
0077' 1A          LXI  D,HIRAM        ; HIGHEST ADDRESS TO CLEAR
0078' 77          LXI  H,LDROM        ; LOWEST ADDRESS TO CLEAR
0079' 13          CLR   H,0      ; CLEAR
007A' 23          JNZ   H,0      ; NOT OVER YET
007B' 05          MOV   H,D  ; GET LOW ORDER BYTE
007C' C2 0077'  CMP   H,D  ; IS IT THE ONE?
007D'          0082' 21 102F  JNZ   H,0      ; NO, KEEP CLEARING
0085' 0085' 36 00          MOV   H,0      ; NO, KEEP CLEARING
0087' 23          INX   H      ; SET UP STACK POINTER
0088' 7A          MOV   H,D  ; SET UP STACK
0089' 8C          CMP   H,D  ; SET UP STACK
008A' C2 0085' 008A' 7F          MOV   H,D  ; SET UP STACK
008B' B0          CMP   H,D  ; SET UP STACK
008C' C2 0085' 008A' 7F          MOV   H,D  ; SET UP STACK
008D'          0092' 31 112F  LXI  H,TRB  ; POINT TO START OF TERMINAL BUFFER AREA
                                                ; INITIALIZE LINE BUFFER VARIABLES
0095' 21 112F  SHLD  H,LBRA        ; CURRENT LINE BUFFER ENTRY
0098' 22 1043  SHLD  CLBE        ; OLDEST TERMINAL BUFFER ENTRY
009B' 22 1045  SHLD  OLRE        ; OLDEST LINE BUFFER ENTRY
009E' 22 1041  SHLD  LRPE        ; LINE BUFFER PROCESSING ENTRY
00A1' 21 1132  LXI  HALBA3        ; POINT TO END OF HEADER AREA
00A4' 22 1047  SHLD  LRIP        ; LINE BUFFER INPUT POINTER
                                                ; INITIALIZE CONNECT BUFFER
00A7' 21 1897  LXI  H,CRF        ; POINT TO START OF TERMINAL BUFFER AREA
00AA' 22 1035  SHLD  OTRE        ; OLDEST TERMINAL BUFFER ENTRY
00AB' 22 1033  SHLD  CTBIE       ; SET UP CURRENT TERMINAL BUFFER INPUT ENTRY ADDRESS
00B0' 23          INX   H      ; INCREMENT ADDRESS BY ONE
                JNZ   H,CTBIE       ; TO POINT TO END OF HEADER
00B1' 22 1037  SHLD  TBIP        ; TERMINAL BUFFER INPUT POINTER
                                                ; LENGTH OF INITIALIZATION DATA
00B4' 21 1061  LXI  H,CRF        ; INITIALIZE CONNECT BUFFER
00B7' 11 0000#  LXI  H,RTRMIF    ; RTRMIF
00C0' 06 08      MUL  R,B      ; B-- LENGTH OF INITIALIZATION DATA

```

Remainder unchanged ...

```

Terminal Node Controller Down-line Loader. MACRO-90 3.36 17-Mar-80 PAGE 1-1
TTF DOWN LINE LOADER
NAME ( TLDL00 )
PAGE 60

; INCLUDE 8250.REF
; 8250 SERIAL I/O EQUATES
; .LIST
; INCLUDE CCAEXT.REF
; COMMON COMMUNICATIONS AREA EXTERNAL DECLARATIONS
; .LIST

BAUDAT EQU BAUD96
FORMAT EQU WLSI4FENSTR ;ASR33

PAGE PGSIZ

; Initialization.
ENTRY MLLD0
ENTRY FLASH0,FLASH1,FLASH2,FLASH3,FLASH4
EXTRN ACTRAM,LCR

; initialize stack pointer to top of ram
MLLD0: LXI SP,STACK
MOV A,DAB
MOV OUT LCR
; set line control bits for UART to set DFG
; set USART line
MOV OUT BAUDAT
OUT BLS
; set LSB of divisor
MOV OUT BAUDAT
; set MSB of divisor
; set it
MOV OUT DLM
; fix up line control DFG bit
MOV OUT LCR

; Now signify proper reset condition by flashing LED on SOUT line
FLASH0: ANI #06
CALL ,,LO1
CALL FLASHB
B
,LO1
JNZ ,,LO1

; * SIGNIFIES START THE LOADER
START: CALL CHRN
CPI '#'
; * SIGNIFIES START PROGRAM
JZ ACTRAM
CPI '#'
START
JNZ ; IF NOT #, TRY AGAIN

; SIGNIFIES START THE LOADER
; READ A BYTE (2 CHARACTERS AND PACK)
LDR0: CALL RBYTE
CPI 00
JZ START
; 0 IS EOF
MOV E,A
; SAVE IN BYTE COUNT
; SAVE IN CHECKSUM
; GET ADDRESS MSR
CALL RBYTE
MOV H,A
ADD D
; ADD IN CHECKSUM
MOV D,A
; REPLACE IT
CALL RBYTE
; GET ADDRESS LSR
MOV L,A
ADD D
; ADD IN CHECKSUM
MOV D,A
; REPLACE IT
CALL RBYTE
; IGNORE ON BYTE

; SET A DATA BYTE
LOADIT: CALL RBYTE
MOV N,A
; STORE IT IN MEMORY
ADD D
; ADD THE CHECKSUM
REPLACE IT
MOV D,A
; POINT AT NEXT LOCATION
INX H
; INCREMENT DATA BYTE COUNTER
INC E
; AND CONTINUE TILL ALL BYTES RECEIVED
; FETCH THE CHECKSUM BYTE
JNZ LOADIT
CALL RBYTE

```

Terminal Node Controller Down-line Loader, TIP DOWN LINT LOADER MACRO-80 3.16 17-Mar-90 PAGE 1-2

```

0050' SF MOV E,A ;PUT COMPUTED CHECKSUM INTO A<CR>
0051' 7A MOV A,D ;TWO'S COMP IT
0052' 2F CMA A ;...
0053' 3C INR E ;SAME AS RECEIVED CHECKSUM ?
0054' BB CMP E ;DIVERGENT Y NOT
0055' C2 008C JNZ ERROR ;LOOK FOR 'C' (SKIP CR,LF)
0056' CD 0080 ..L02: CALL CHRIN
0057' FE 3A CPI ;;
0058' C2 0058' JNZ ..L02 ;GO TO BEGINNING FOR NEXT RECORD
0059' 0040' JMP LOADER ;LOADER

; UTILITIES
0063' C5 RBYTE: PUSH B ;READ 2 BYTES AND PACK TO ONE REAL
0064' CD 0072' CALL RHEX
0065' 07 RLC B,A ;MOV D,A
0066' 07 RLC CALL RHEX
0067' 07 RLC DRA B ;CALL RHEX
0068' 07 RLC POP B ;DRA B
0069' 07 RLC RET ;POP B
006A' 07 RLC ;RET
006B' 47 RHEX: CALL RHEX
006C' CD 0072' RET ;RET
006F' B0 RHEX: CALL RHEX
0070' C1 POP B ;POP B
0071' C9 RET ;RET

0072' CD 0080' ;READ A HEX MIRBLE
0073' FE JA RRDIG ;IS IT A DIGIT
0077' DA 007B' JC RRDIG ;YES, TURN INTO BINARY
007A' B6 37 SUI 'A'-10 ;ASSUME A-F, MAKE BINARY
007C' C9 RET ;RET
007D' D6 30 RRDIG: SUI '0' ;MAKE DIGIT BINARY
007E' C9 RET ;RET

0080' D8 05 CHRIN: IN LSR ;READ FROM UART STATUS
0082' E6 01 ANI 1 ;CHECK READY
0084' CA 0080' JZ CHRIN ;NOT YET.
0087' DB 00 IN RBR ;READ CHARACTER
0089' E6 7F ANI 07FH ;MASK TO 7 BITS
008B' C9 RET ;RET

008C' CD 00AD' ;FLASHD
008E' C3 008C' JMP ERROR ;FLASH CONTINUOUSLY ON ERROR

0092' 3E 40 FLASHA: INI A,040H ;MAKE SOUT LOW TO TURN LED ON
0094' 30 SIM 0040H ;TURN IT ON
0095' CD 0003' CALL DELAY ;WAIT A BIT
0098' F6 80 ORI 080H ;RAISE SOUT LINE TO TURN LED OFF
009A' 30 SIM 0040H ;DO IT
009B' CD 0003' CALL DELAY ;WAIT
009E' C9 RET ;RET

009F' JE 08 FLASHB: INI A,0072H ;GET BIT FOR OUT2 LED ON B250
00A0' D3 04 OUT MCR ;OUT
00A3' CD 0003' CALL DELAY ;A
00A6' AF XRA ;XRA
00A7' D3 04 OUT MCR ;OUT

```

Terminal Node Controller Down-line Loader, TIP DOWN LINT (04) MACRO-80 3.16 17-Mar-90 PAGE 1-3

```

; GET COMMAND SEQUENCE FOR LED 'D' ON ON 8273
00A8' CD 0003' CALL RFT ;CALL
00A9' C9 ;FLASHB: LXI H,CMD3 ;GET COMMAND FOR LED 'E' ON
00AC' C9 ;CALL CMOUT ;CALL
00B0' CD 0000H ;CALL DELAY ;LXI H,CMD4 ;LED 'D' OFF
00B3' CD 0003' CALL CMOUT ;CALL
00B6' 21 00E9' CALL DELAY ;CALL
00B9' CD 0000H ;CALL RET ;RET
00C0' CD 0003' CALL CMOUT ;CALL
00C3' CD 0000H ;CALL DELAY ;CALL
00C6' CD 0003' CALL CMOUT ;CALL
00C9' 21 00E3' CALL DELAY ;LXI H,CMD2 ;COMMAND LED 'E' OFF
00CC' CD 0000H ;CALL CMOUT ;CALL
00CF' CD 0013' CALL DELAY ;CALL
00D2' C9 ;RET ;RET
00D3' 26 32 ;DELAY: MVI H,50
00D5' 2E 00 ;MVI L,0
00D7' 2D ;MVI L,04; DCR L
00D8' C2 0007' ;JNZ ..L04 ;DCR H
00D9' 25 ;JNZ ..L03 ;DCR H
00DA' C2 0005' ;JNZ ..L03 ;DCR H
00DB' C9 ;RET ;RET

; COMMAND FOR LINES ON AND OFF
00E0' 01 A3 10 ;CMD1: 1,063H-010H
00E3' 01 63 EF ;CMD2: 1,063H-0EFH
00E6' 01 A3 08 ;CMD3: 1,043H-08H
00E9' 01 63 F7 ;CMD4: 1,063H-0F7H
;REALITY
;END

;READ FROM UART STATUS
;CHECK READY
;NOT YET.
;READ CHARACTER
;MASK TO 7 BITS
;FLASHD
;FLASH CONTINUOUSLY ON ERROR
;FLASHB: INI A,040H ;MAKE SOUT LOW TO TURN LED ON
;TURN IT ON
;WAIT A BIT
;RAISE SOUT LINE TO TURN LED OFF
;DO IT
;WAIT
;FLASHB: INI A,0072H ;GET BIT FOR OUT2 LED ON B250
;OUT MCR ;OUT
;CALL DELAY ;A
;XRA ;XRA
;OUT MCR ;OUT

```

* - PEOPLE AT JAN 25TH MEETING

Write code primarily in C.

Frank Roberts,

VE3FAO

27 Willis Dr.,

Brampton,

Ontario,

L6W 1A8.

*
*

>TYPE MAILLIST.
** DMO:1,76MAILIST;:21 -- Last written 26-JAN-81 14:49:16 **

*** Robert Sleath,
1275 Elsin St., #1402,
Burlington, Ontario.

H 632-6279 0 637-4515
+ 64 character display, terminal only. Runs off
Yessu synthesized walkie. Mini monitor in terminal
node. Uses parallel interface to keyboard and display.
Interested in packet voice and access to other computer
systems.

*** Brian Kennedy,
90 Sarah Lane, Unit #3,
Oakville, Ontario,
L6L 5L3.

+ H 825-0925 0 865-4427
TRS-80 system.

*** AMRAD Corp.,
1524 Spring Vale Avenue,
McLean, Virginia, 22101.

+ SWP bulletins
*** Dr. Thomas A. Dwyer,
Solidworks Laboratory,
Dept. Computer Science,
University of Pittsburgh,
Pittsburgh, PA, 15260.

*** distributed applications a la N-TREK.
send information re multi-user implementations.

*** John Vender Rerg,
RR #2, Group 6, Box 14,
Mount Hope, Ontario,
LOR 1M0.

*** H 692-3802 0 528-8447
Down loadable terminal node on homebrew Z-80 CP/M system.
Super monitor package for monitoring and running
the TNC. Has remote console on his system.
interested in Digital Picture transmission and graphics.

*** Stewart Best,
2391 Arnold Cres.,
Burlington, Ontario,
L7P 4J2.

+ H 335-3033 0 528-8811 x4242
TNC board nearing completion. TRS-80 system.

+ *** Fulko Hew,
6650 Twiss Road, RR #3,
Campbellville, Ontario,
LOF 1R0.

*** Glenn Simpson,
61 Briarwood Cres.,
Hamilton, Ontario,
L9C 4C3.

+ H 385-8478 0 528-0811 x3122
TNC nearing completion. TRS-80 and 1602 system.
Interested in satellite links and (later) packet
voice.

*** Dan Robertson,
32 George Henry Blvd.,
Willowdale, Ontario,
M2V 1E2.

+ H 494-7288 0 499-5050
MCW-800 APL machine, interested in CRSS

*** W.J.Montgomery,
VE3EC

*
*

8 McCordick Drive,
St. Catharines, Ontario,
L2N 6S3.
+ H 934-6303 0 637-4515
TNC on CP/M system. Interested in Color interactive
graphics, file transfer. Uses C and Pascal
\$\$\$ James Knott, VE3CVM
55 Park St., #1402,
Mississauga, Ontario,
L5G 1L9.
+ H 279-5399 0 860-5183
Imssai 8080 cassette system. Works for CN/CP
servicing TTY equipment.
\$\$\$ Paul Deversaux,
1337 Woodvale Place,
Burlington, Ontario,
L7R 1Y9.
+ Programmer. Interested in network.
\$\$\$ Michael Connolly, VE3MDC
34 Schubert Drive,
Scarborough, Ontario,
M1E 1Y9.
+ H 281-0513 0 966-5575
With DOC residential office, Toronto. responsible for
training radio inspectors. believes we should provide
a standardized protocol among all experimenters
rather than isolated cells.
\$\$\$ Russel S. Milland,
12 Princess Margaret Blvd.,
Etobicoke, Ontario,
M9A 1Z4.
+ H 231-0252 0 968-4838
Z-80 S-100 system running CP/M and PL-1.
designed digital systems as engineer, now interested in
RTTY, HF experiments, CRSS.
\$\$\$ Dr. George Piszecki, VE3GUH
473 Copeland Court,
Oakville, Ontario,
L6J 4R8.
+ H 844-9889 0 844-2444
PET machine with dual floppy. interested in CBRS.
Member of rather large PET computer club.
\$\$\$ Tom Gleeson, VE3MFU (W9ITI)
+ member of PET club.
\$\$\$ Keith Witney, VE3DYM
740 York Mills Rd., #1508,

Don Mills, Ontario.
+ cannot locate this person.
\$\$\$ Clayt Anduish, VE3LU
900 Colborne St.,
Brantford, Ontario.
+ H (519) 753-7674
\$\$\$ Glen Leinweber,
110 Marlboro Dr.,
Hamilton, Ontario,
L9C 2H9.
+ H 389-5658 0 525-9140 x4251
IMSAI 8080 system currently used for processing weather
satellite Pictures. interested in graphics and high-speed
communication.
\$\$\$ Ray Ewan, VE3HWY
1058 Joan Drive,
Burlington, Ontario,
L7T 3H2.
+ H 634-1712
S-100 Z-80 system with 1 floppy and 9T tape.
CP/M 1.4
\$\$\$ Brian Fox, VE3FRF
45 Rosedale,
Gainsby, Ontario.
+ H 945-8179 0 561-9311
\$\$\$ Jeff Knight,
141 Castlerock Dr.,
House #42,
Richmond Hill, Ontario,
L4C 5N2.
+ H 884-3299 0 860-2876
AIM-65 system.
\$\$\$ Al Lightstone,
89 German Mills Rd.,
Thornhill, Ontario,
L3T 4H9.
+ H 889-9657 0 223-8191
On board of directors RSO. AIM-65 system
interested in CBRS and satellite (Phase 3R)
>

Application Note

AN-01

三

THE AR-220 / FSK MODULATION

Stable F5K Models Reborn!!! And Now, With More Options!!!

- Stable FSK Modems Featuring the XR-2207, XR-2206 and XR-2211**

 - Phase-continuous FSK output
 - Provides both triangle and squarewave outputs
 - Operates single-channel or two-channel mode
 - Inputs are TTL and C/MOS compatible

This Applications Note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application.

The devices featured in this Application Note are the XR-2206 and XR-2207 FSK modulators, and the XR-2211 FSK demodulator with carrier-detect capability. Because of the superior frequency stability (typically 20 ppm/ $^{\circ}$ C) of these devices, a properly designed modem using them will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this Applications Note can be used with mark and space frequencies anywhere from several Hertz to 100 kiloHertz.

THE AK-2200 ISK MODULATOR

THERMALS

- Choice of 0.5% THD sinewave, triangle output
 - Phase-continuous FSK output
 - Inputs are TTL and CMOS compatible
 - Low power supply sensitivity ($0.01\%/\text{V}$)
 - Split or single supply operation
 - Low external parts count

The output impedance at pin 2 is about 600Ω with AC coupling normally be used.

pins 13 thru 16 may be left open-circuited.

total harmonic distortion. In applications where minimal distortion is unnecessary, pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor. In applications where a triangular output waveform is satisfactory,

shows split-supply operation. When used as an FSK modulator pins 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and CMOS logic forms. When used with single supply, the threshold is near mid-supply and is CMOS compatible. Table I shows how to select the timing resistors R_1 thru R_4 to determine the output frequency based upon the logic levels applied to pins 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10 k Ω and 100 k Ω .

With pin 8 grounded, pin 9 serves as the data input. A high-level signal applied to pin 8 will disable the oscillator. When used in this manner, pin 8 of the XR-2207 serves as the channel-select input. For two-channel multilevel operation, pins 4 and

channel operation, pins 4 and 5 should be left open-circuited.)

DISCUSSION

The XR-2208 is ideal for FSK applications requiring the spectral purity of a sinusoidal carrier waveform. It offers TTI and

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to pin 9. A high level signal selects the frequency ($1/(R_7C_1)$) Hz; a low level signal selects the frequency ($1/(R_7C_3)$) Hz. (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10 k Ω to 100 k Ω . The voltage applied to pin 9 should be selected to fall between ground and +4.05%. If left untrimmed, it is approximately 2.5%.

TABLE I
XR-2207 FSK Input Control Logic

Logic Level	Active Timing Resistor	Output Frequency
High	Resistor 1	Low

Figure 3. The XR-2207 FSK Modulator Split-Supply Operation

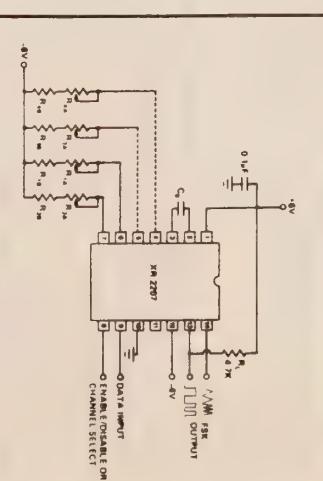
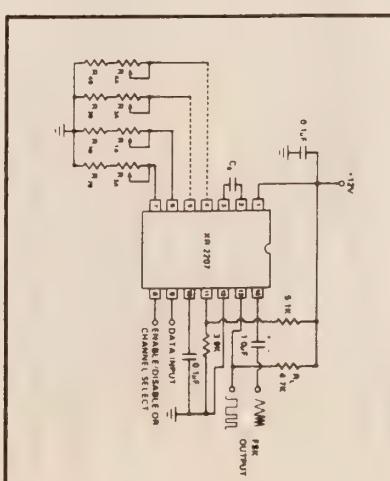


Figure 2 The AK-220 FSK Modulator Single-Supply Operation



THE XR-2211 FSK DEMODULATOR WITH CARRIER DETECT

FEATURES

- Typically 20 ppm/ $^{\circ}\text{C}$ temperature stability
- Simultaneous FSK and carrier-detect output
- Outputs are TTL and C/MOS compatible
- Wide dynamic range (2 mV to 3 VRMS)
- Split or single supply operation
- Low power supply sensitivity (0.05%/V)
- Low external parts count

OPERATION

The XR-2211 is a FSK demodulator which operates on the phase-locked-loop principle. Its performance is virtually independent of input signal strength variations over the range of 2 mV to 3 VRMS.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_0 = (1/C_1 R_1) \text{ Hz}$, where capacitance is in farads and resistance is in ohms. R_0 should be calculated to fall midway between the mark and space frequencies.

The XR-2211 has three NPN open collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output. Pin 5 is the Q lock-detect output, which goes low when a carrier is detected, and Pin 6 is the \bar{Q} lock detect output, which goes high when lock is detected. If pins 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied and will be "low" when no carrier is present.

If the lock-detect feature is not required, pins 3, 5 and 6 may be left open-circuited.

The tracking range (Δf) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_1 f_0 / R_2) \text{ Hz}$. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10 k Ω and 100 k Ω .

The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2 , which, in conjunction with R_5 , forms the loop filter time constant. In most modem applications, $\Delta f_c = (80\% - 99\%) \Delta f$. The loop damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. It is determined by $\zeta = \frac{1}{2}\sqrt{C_1/C_2}$. For most modem applications, choose $\zeta \approx \frac{1}{2}$.

DESIGNING THE MODEM

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency. (Less than a 2:1 ratio)
- For minimum demodulated output pulselwidth jitter, select an FSK band whose mark and space frequencies are

- both high compared to the baud rate. (i.e., for a 300 baud channel, mark and space frequencies of 2025 Hz and 2225 Hz would result in significantly less pulselwidth jitter than 300 Hz and 550 Hz).
- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship mark-space frequency difference (Hz) $> 83\%$ maximum data rate (baud) should be observed.

TABLE 2
Recommended Component Values for Typical FSK Bands

FSK Band				XR-2207				XR-2206				XR-2211							
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	C_0	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D	
300	1070	1270	10	20	100	0.39	10	18	10	20	0.39	10	18	100	0.39	.01	.005	.05	
300	2025	2225	10	18	150	0.60	0.22	10	16	10	18	0.22	10	18	200	0.22	.0047	.005	
1200	1200	2200	20	30	20	0.36	0.22	10	16	20	30	0.22	10	18	30	0.27	.01	.0022	

Units: Frequency - Hz, Resistors k Ω ; Capacitors μF

DESIGN EXAMPLES

- A. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

1. Frequency Calculation

Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore choose an upper frequency:

$$\frac{83 \times 10,000}{45} = 18,444 \text{ kHz} \approx 18.5 \text{ kHz.}$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10,175 \text{ kHz.}$$

2. Component Selection

- a. To calculate R_3 , we first need our Δf , which is $18,500 - 10,175$, or 8,325 kHz. Now, select a value of C_0 to generate 10,175 kHz with R_1 :

$$R_3 = (25,800 \times 14,338)/R_3; \\ R_3 = 44.4 \text{ k}\Omega \approx 47 \text{ k}\Omega.$$

- b. To determine C_2 use $\zeta = \frac{1}{2}\sqrt{C_1/C_2}$. Then, $C_2 = \frac{1}{4}C_1; C_2 = 670 \text{ pF}$.

- c. To select C_F , we use $\tau_F = [0.3/(\text{baud rate})]^{1/2}$. $1/C_0 R_2; R_2 = 36 \text{ k}\Omega$.

A good choice would be to use 10 k Ω potentiometers for the FSK band whose mark and space frequencies are

$\tau_F = 0.3/10,000 = 30 \text{ }\mu\text{sec.}$; with $R_F = 100 \text{ k}\Omega, C_F = 300 \text{ pF}$.

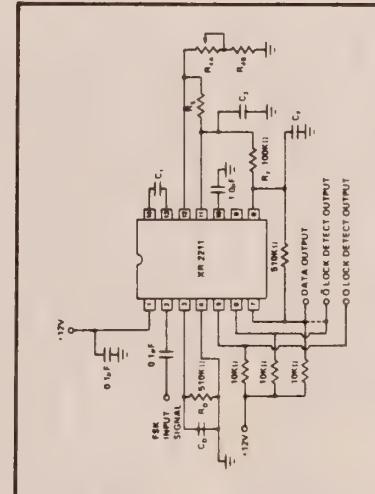


Figure 4. The XR-2211 FSK Demodulator with Carrier Detect

- a. For the XR-2207 FSK modulator, set $R_1 \approx 30 \text{ k}\Omega$. Now, select a value of C_0 to generate 10,175 kHz with R_1 :

- b. To determine C_2 use $\zeta = \frac{1}{2}\sqrt{C_1/C_2}$. Then, $C_2 = \frac{1}{4}C_1; C_2 = 670 \text{ pF}$.

- c. To select C_F , we use $\tau_F = [0.3/(\text{baud rate})]^{1/2}$. $1/C_0 R_2; R_2 = 36 \text{ k}\Omega$.

A good choice would be to use 10 k Ω potentiometers for the FSK band whose mark and space frequencies are

- $\tau_F = 0.3/10,000 = 30 \text{ }\mu\text{sec.}$; with $R_F = 100 \text{ k}\Omega, C_F = 300 \text{ pF}$.

Here are several guidelines to use when calculating non-standard frequencies:

4. Lock Range Selection

To select C_D , let us start with the actual lock range:

$$\Delta f = R_4 f_0 / R_3 \text{ Hz} = 7870 \text{ Hz}$$

If we assume a capture range of 80%,

$$\Delta f_C = 6296 \text{ Hz},$$

therefore, our total capture range or Δf_C is 12,592 Hz.

Our minimum value for C_D is $(16/12,592) \mu\text{f}$ or $0.0013 \mu\text{f}$.

5. Completed Circuit Example

See Figure 5.

- B. Design a 3 kilobaud modem to operate with low output jitter.** The bandwidth available is 13 kHz.

For this modem, we can take the values from 2 for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by 10, and divide all capacitor values on the table by 10. Resistor values should be left as they are.

- C. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 and 1700 Hz. (Each of these channels could handle about 400 baud.)**

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 k Ω and 100 k Ω : R_1 , R_2 / R_3 , R_3 and R_4 . The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 k Ω , we have $1700 = 1/(C_0 \times 20,000)$; $C_0 = 0.029 \mu\text{f}$ which is approximately equal to 0.033 μf .

ADJUSTMENT PROCEDURE

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on pin 9. Then with a high level on pin 9, adjust the high frequency using R_{2B} or R_{4B} . The second adjustment affects only the high frequency, whereas the first adjustment affects both the low and the high frequencies.

The XR-2206: The upper and lower frequency adjustments are independent so the sequence is not important.

The XR-2211: With the input open-circuited, the loop phase detector output voltage is essentially undefined

Calculating R_1 using 600 Hz and 0.033 μf , we get $R_1 = 50.5 \text{ k}\Omega$. We can use $R_{1B} = 47 \text{ k}\Omega$ and $R_{1A} = 10 \text{ k}\Omega$.

For R_2 , we get 101 k Ω . Use $R_{2B} = 91 \text{ k}\Omega$ and $R_{2A} = 20 \text{ k}\Omega$. To determine R_3 , use: $1400 \text{ Hz} = 1/R_3 C_0$, which gives us $R_3 = 21.6 \text{ k}\Omega$. Use $R_{3B} = 18 \text{ k}\Omega$ and $R_{3A} = 5 \text{k}\Omega$. R_4 must generate a 300 Hz shift in frequency, the same as R_2 . Therefore set R_4 equal to R_2 .

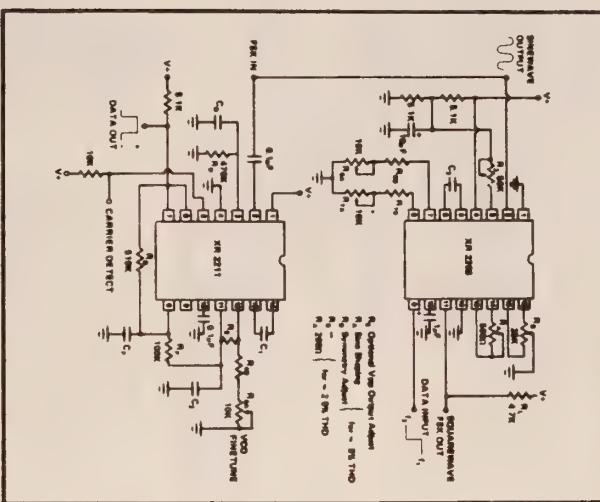


Figure 5. Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

XR-2211

FSK Demodulator/Tone Decoder

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier-Detection	
Wide Dynamic Range	
Adjustable Tracking Range ($\pm 1\%$ to $\pm 80\%$)	
Excellent Temp. Stability	20 ppm/ $^{\circ}\text{C}$, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM R RATINGS

Part Number	Power Supply	Operating Temperature
XR-2211M	3V rms	-55°C to +125°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C
XR-2211IP	Ceramic	-40°C to +85°C
	Plastic	-40°C to +85°C

AVAILABLE TYPES

Part Number
XR-2211M
XR-2211CN
XR-2211CP
XR-2211IP

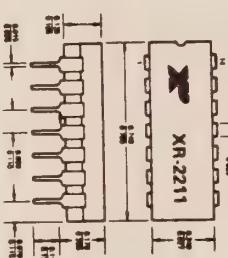
Package
Ceramic
Plastic
Ceramic
Plastic

Power Dissipation
750 mW
6 mV/ $^{\circ}\text{C}$
625 mW
5.0 mW/ $^{\circ}\text{C}$

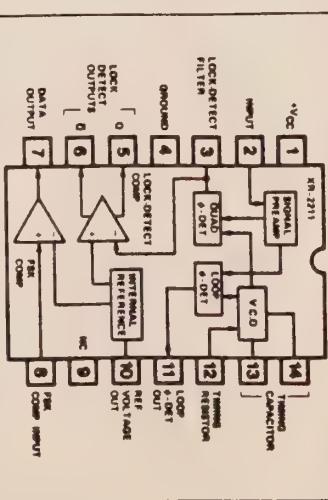
Ceramic Package:
Derate above $T_A = +25^{\circ}\text{C}$

Plastic Package:
Derate above $T_A = +25^{\circ}\text{C}$

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25^\circ C$, $R_0 = 30 k\Omega$, $C_0 = 0.033 \mu F$. See Fig. 2 for component designation

CHARACTERISTICS	XR-2211/2211M			XR-2211C			CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
GENERAL							
Supply Voltage	4.5	4	20	4.5	5	20	V mA
Supply Current							$R_0 \geq 10 k\Omega$. See Fig. 4
OSCILLATOR SECTION							
Frequency Accuracy		± 1	± 3				% Deviation from $f_0 = 1/R_0 C_0$
Frequency Stability		± 20	± 50	± 0.05	± 0.05	± 0.2	$R_1 = \infty$ ppm/ $^\circ C$ See Fig. 8.
Temperature	0.05	0.5	0.2	0.2	0.2	300	%/V $V^+ = 12 \pm 1 V$. See Fig. 7.
Power Supply	100	300	1000	0.01	0.01	0.01	%/V $V^+ = 5 \pm 0.5 V$. See Fig. 7. kHz $R_0 = 8.2 k\Omega$, $C_0 = 400 pF$
Upper Frequency Limit							
Lowest Practical							
Operating Frequency							
Timing Resistor, R_0							$H_z = 2 M\Omega$, $C_0 = 50 \mu F$ See Fig. 5.
Operating Range	5	2000	5	2000	5	100	KHz KΩ KΩ KΩ See Fig. 7 and 8.
Recommended Range	15	100	15	100	15	100	
LOOP PHASE DETECTOR SECTION							
Peak Output Current	± 150	± 200	± 300	± 100	± 200	± 300	μA μA $M\Omega$ V_{pp}
Output Offset Current		± 1			± 2		Measured at Pin 11.
Output Impedance		1	1		1		Measured at Pin 10.
Maximum Swing		± 4	± 5	± 4	± 5		Measured at Pin 3.
QUADRATURE PHASE DETECTOR							
Peak Output Current	100	150	1	150	1	1	μA $M\Omega$ V_{pp}
Output Impedance		11	11		11	11	Measured at Pin 2.
Maximum Swing							$k\Omega$ mV_{rms}
INPUT PREAMP SECTION							
Input Impedance		20	20		20	20	
Input Signal		2	10		2	2	
Voltage Required to Cause Limiting							
VOLTAGE COMPARATOR SECTIONS							
Input Impedance		2	2		2	2	$M\Omega$ nA dB mV μA
Input Bias Current	100	100	100	55	70	300	Measured at Pins 3 and 8.
Voltage Gain	70	70	70	300	300	.01	$R_L = 5.1 k\Omega$ $I_C = 3 mA$ $V_O = 12V$
Output Voltage Low	300	300	300				
Output Leakage Current	.01	.01	.01				
INTERNAL REFERENCE							
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance		100	100		100	100	Ω

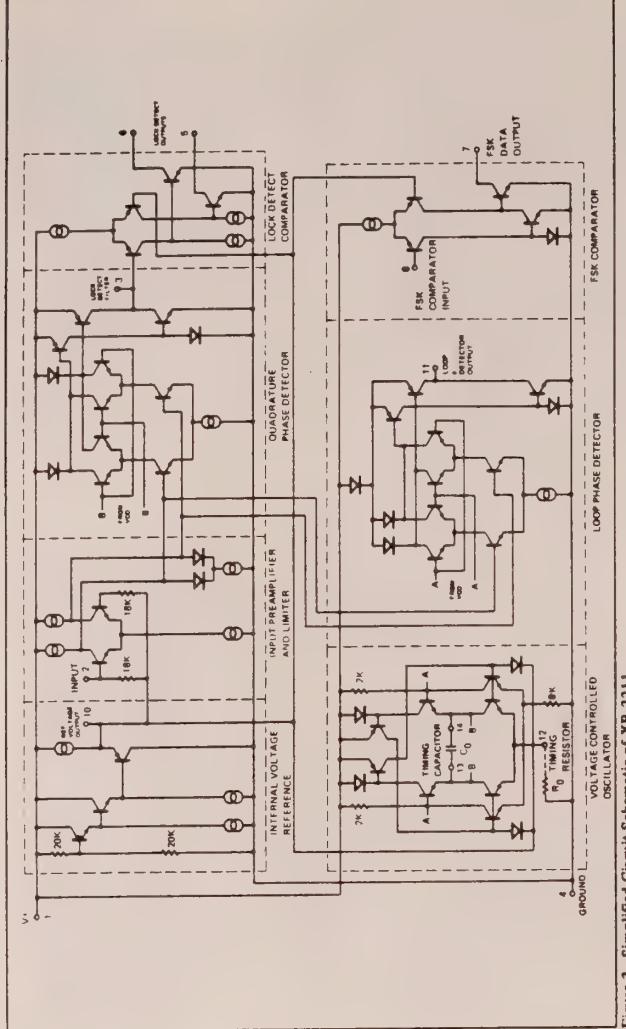


Figure 3. Simplified Circuit Schematic of XR-2211.

TYPICAL CHARACTERISTICS

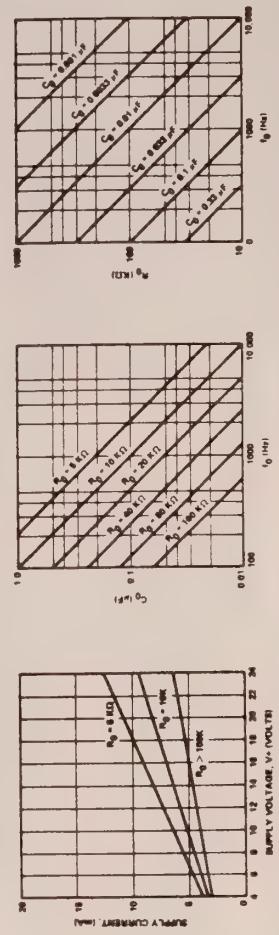


Figure 4. Typical Supply Current vs V^+ (Logic Outputs Open Circuited).

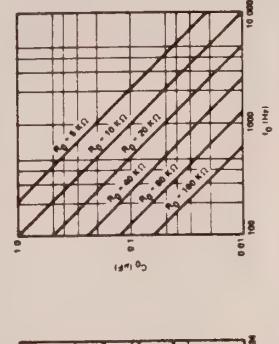


Figure 5. VCO Frequency vs Timing Resistor

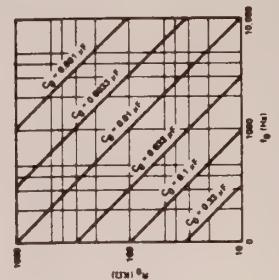


Figure 6. VCO Frequency vs Temperature

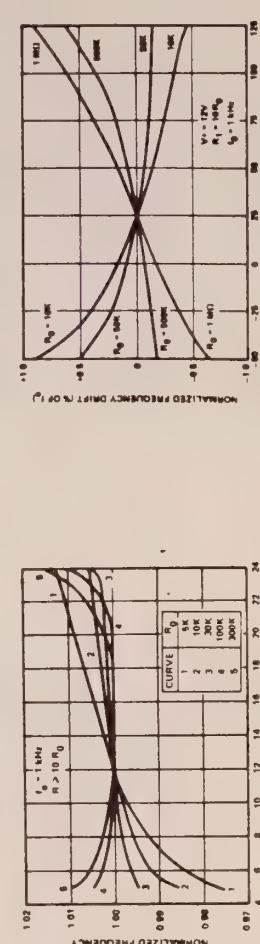


Figure 7. Typical f_0 vs Power Supply Characteristics.

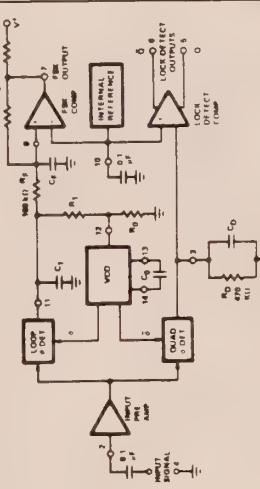


Figure 8. Generalized Circuit Connection for FSK and Tone Detection.

FUNCTIONAL BLOCK DIAGRAM

Test Conditions: $V^+ = +12V$, $T_A = +25^\circ C$, $R_0 = 30 k\Omega$, $C_0 = 0.033 \mu F$. See Fig. 2 for component designation

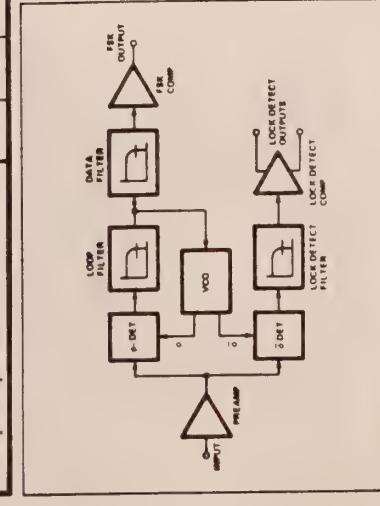
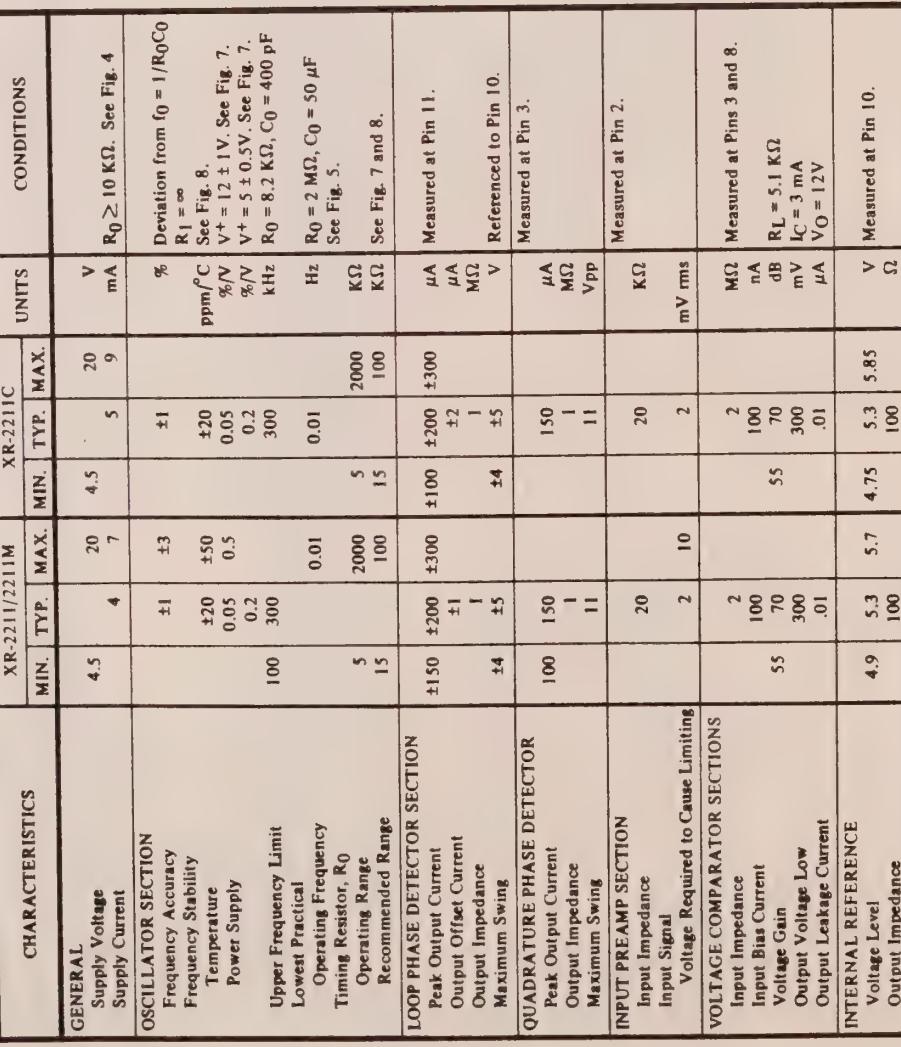


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 K Ω . Recommended input signal level is in the range of 10 mVrms to 3 Vrms.

Quadrature Phase Detector Output (Pin 3): This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (See Fig. 2) to eliminate the chatter at lock-detect outputs. If the tone-detect section is not used, Pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, R_L, to V₊ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock-Detect Complement, \bar{Q} (Pin 6): The output at Pin 6 is the logic complement of the lock-detect output at Pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open-collector logic stage which requires a pull-up resistor, R_L, to V₊ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection data filter is connected between this terminal and the PLL phase-detector output (Pin 11). This data filter is formed by RF and CF of Fig. 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: V_R = V₊/2 - 650 mV.

The dc voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 μ F capacitor, for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R₁ and C₁ connected to Pin 11 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to ΔV_R .

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R₀, connected from this terminal to ground. The VCO free-running frequency, f₀, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C₀ is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R₀ must be in the range of 10 K Ω to 100 K Ω (See Fig. 8).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C₀. Connected across these terminals (See Fig. 5), C₀ must be non-polar, and in the range of 200 pF to 10 μ F.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R₀ at Pin 12 (See Fig. 9).

VCO Free-Running Frequency, f₀: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

DESIGN EQUATIONS
(See Fig. 2 for Definition of Components)

1. VCO Center Frequency, f₀:

$$f_0 = 1/R_0 C_0 \text{ Hz}$$

2. Internal Reference Voltage, V_R (measured at Pin 10)

$$V_R = V_+/2 - 650 \text{ mV}$$

3. Loop Low-Pass Filter Time Constant, τ :
 $\tau = R_1 C_1$

4. Loop Damping, ξ :

$$\xi = 1/4 \sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
 $\Delta f/f_0 = R_0/R_1$

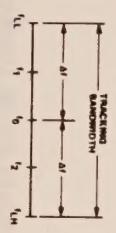


Figure 9. Circuit Connection for FSK Decoding

Design Instructions:

The circuit of Fig. 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R₀, R₁, C₀, C₁ and CF. For a given set of FSK mark and space frequencies, f₁ and f₂, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f₀:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R₀, to be in the range of 10 K Ω to 100 K Ω . This choice is arbitrary. The recommended value is R₀ \geq 20 K Ω . The final value of R₀ is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C₀ from design equation (1) or from Fig. 6.

$$C_0 = 1/R_0 f_0$$

d) Calculate R₁ to give a Δf equal to the mark-space deviation:

$$R_1 = R_0 [f_0(f_1 - f_2)]$$

e) Calculate C₁ to set loop damping. (See Design Equations No. 4).

Normally, $\xi \approx 1/2$ is recommended.

Then: C₁ = C₀/4 for $\xi = 1/2$

i) Calculate Data Filter Capacitance, C_F:
For R_F = 100 K Ω , R_B = 510 K Ω , the recommended value of C_F is:
 $C_F \approx 3/(\text{Baud Rate}) \mu\text{F}$

9. Total Loop Gain, K_T:

$$K_T = 2K_F K_0 = 4/R_0 R_1 \text{ rad/sec/volt}$$

Note: All calculated component values except R₀ can be rounded-off to the nearest standard value, and R₀ can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Fig. 9).

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R₀ and C₀ set the PLL center frequency, R₁ sets the system band width, and C₁ sets the loop filter time constant and the loop damping factor. CF and RF form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 K Ω) from Pin 7 to Pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table I.

TABLE I
Recommended Component Values for Commonly Used FSK Bands (See Circuit of Fig. 9)

FSK BAND	COMPONENT VALUES
300 Baud	C ₀ = 0.039 μ F C ₁ = 0.01 μ F R ₀ = 18 K Ω R ₁ = 100 K Ω
300 Baud	C ₀ = 0.022 μ F C ₁ = 0.0047 μ F R ₀ = 18 K Ω R ₁ = 200 K Ω
1200 Baud	C ₀ = 0.027 μ F C ₁ = 0.01 μ F R ₀ = 18 K Ω R ₁ = 30 K Ω
1200 Baud	C ₀ = 0.0227 μ F C ₁ = 0.0022 μ F R ₀ = 18 K Ω R ₁ = 2200 Hz

Note: All values except R₀ can be rounded-off to nearest standard value.

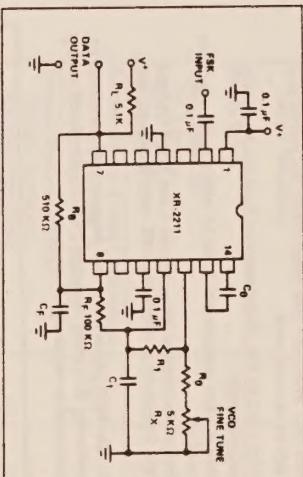


Figure 10. External Connectors for FSK Demodulation with Carrier-Detect Capability.

Note: Data Output is "Low" When No Carrier is Present.

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of C_D will slow the response time of the lock-detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and \bar{Q} at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} , as shown in Fig. 11.

With reference to Figs. 2 and 11, the functions of the external circuit components can be explained as follows: R_Q and C_Q set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low-pass filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and \bar{Q} logic outputs.

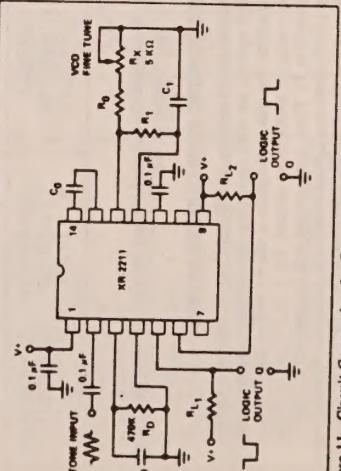


Figure 11. Circuit Connection for Tone Detection

Design Instructions:

The circuit of Fig. 11 can be optimized for any tone-detection application by the choice of the 5 key circuit components: R_Q , R_1 , C_0 , C_1 and C_D . For a given input the tone frequency, f_S , these parameters are calculated as follows:

- Choose R_Q to be in the range of 15 k Ω to 100 k Ω . This choice is arbitrary.
- Calculate C_0 to set center frequency, f_0 equal to f_S (See Fig. 6). $C_0 = 1/(R_Q f_S)$
- Calculate R_1 to set bandwidth $\pm \Delta f$: (see design Equations No. 5):

$$R_1 = R_Q(f_0/\Delta f)^2$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

- Calculate value of C_1 for a given loop damping factor:

$$C_1 = C_0/16f_0^2$$
- Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C_1 = 0.25 C_0$.
- Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.
- Calculate value of filter capacitor C_D . To avoid "chatter" at the logic output, with $R_D = 470\text{ k}\Omega$, C_D must be:

$$C_D(\mu\text{F}) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz \pm 20 Hz:

- Choose $R_Q = 20\text{ k}\Omega$ ($18\text{ k}\Omega$ in series with $5\text{ k}\Omega$ potentiometer).
- Choose C_0 for $f_0 = 1\text{ kHz}$: From Fig. 6: $C_0 = 0.05\text{ }\mu\text{F}$.
- Calculate R_1 : $R_1 = (R_Q)(1000/20) = 1\text{ M}\Omega$.
- Calculate C_1 : for $\zeta = 1/2$, $C_1 = 0.25$, $C_0 = 0.13\text{ }\mu\text{F}$.
- Calculate C_D : $C_D = 16/38 = 0.42\text{ }\mu\text{F}$.
- Fine-tune center frequency with $5\text{ k}\Omega$ potentiometer, R_X .

ADJUSTMENT PROCEDURE

With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_0 can be monitored:

- Short pin 2 to pin 10 and measure f_0 at pin 3 with C_D disconnected;
- Open R1 and monitor pin 13 or 14 with a high-impedance probe; or
- Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

NOTE: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

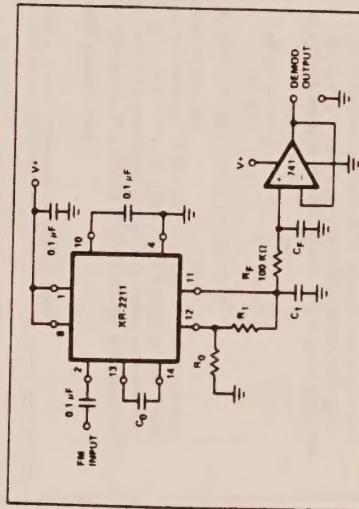


Figure 12. Linear FM Detector Using XR-2211 and an External Op. Amp. (See section on Design Equations, for Component Values)

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F , and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{\text{out}} = R_1 V_R / 100 R_0 \text{ Volts/}\% \text{ deviation}$$

where V_R is the internal reference voltage: $(V_R = V_+/2 - 650\text{ mV})$. For the choice of external components R_1 , R_0 , C_F , C_D , C_1 and C_0 , see section on Design Equations.

Remember:

STATION NODES

145.65 MHz

Point to Point

RAC CHANNEL

146.46 MHz

XR-2206

Monolithic Function Generator

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and noise waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/ $^{\circ}$ C. The oscillator frequency can be linearly swept over a 100 MHz frequency range with an external control voltage with very little effect on distortion.

As shown in Figure 1, the monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level

FEATURES

- Low Sinewave Distortion (THD < .5%) – insensitive to signal sweep
 - Excellent Stability (20 ppm/ $^{\circ}$ C, typ)
 - Wide Sweep Range** (2000:1, typ)
 - Low Supply Sensitivity (0.01%/ V , typ)
 - Linear Amplitude Modulation
 - Adjustable Duty-Cycle (1% to 99%)
 - TTL Compatible FSK Controls
 - Wide Supply Range (10V to 26V)

APPLICATIONS

- Waveform Generation
 - Sine, Square, Triangle, Ramp
 - Sweep Generation
 - AM/FM Generation
 - FSK and PSK Generation
 - Voltage-to-Frequency Conversion
 - Tone Generation
 - Phase-Locked Loops

EQUIVALENT SCHEMATIC DIAGRAM

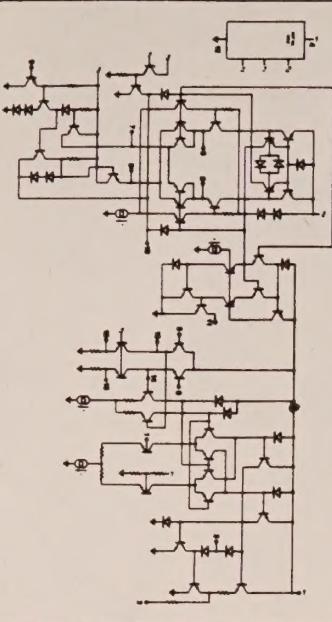
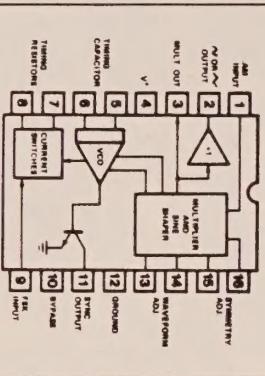
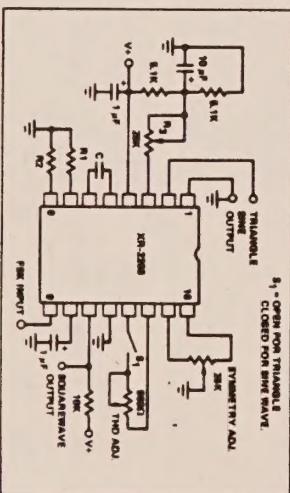


Figure 1.

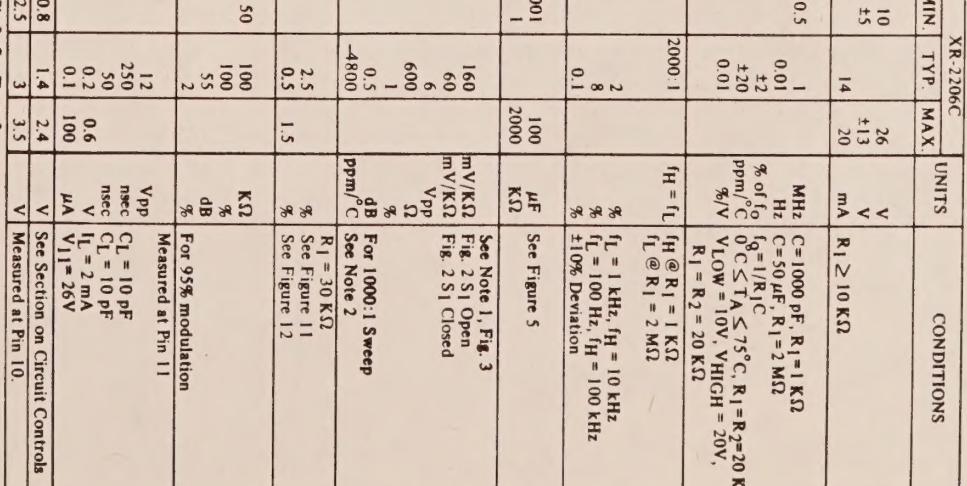


FUNCTIONAL BLOCK DIAGRAM

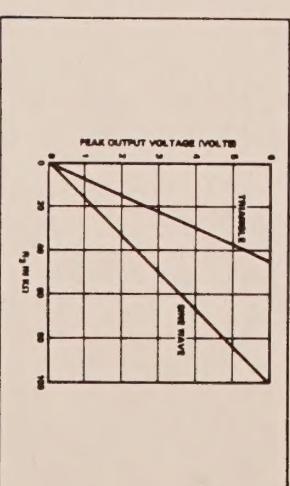
CHARACTERISTICS		XR-2206/XR-2206M		XR-2206C		UNITS	CONDITIONS
MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage	10	26	10	26	26	V	
Single Supply	±5	12	±5	14	±13	V	
Split Supply					20	mA	$R_1 \geq 10 \text{ k}\Omega$
Supply Current							
Oscillator Section							
Max. Operating Frequency	0.5	1	0.5	1	1	MHz	$C = 1000 \text{ pF}, R_1 = 1 \text{ k}\Omega$
Lowest Practical Frequency	0.01	±4	0.01	±2	0.01	Hz	$C = 10 \mu\text{F}, R_1 = 2 \text{ M}\Omega$
Frequency Accuracy	±10	±50	±20	±10	±20	% of f_0	$f_0 = 1/\sqrt{C}$
Temperature Stability	0.01	0.1	0.01	0.01	0.01	ppm/°C	$0^\circ\text{C} \leq TA \leq 75^\circ\text{C}, R_1 = R_2 = 20 \text{ k}\Omega$
Supply Sensitivity						V/V	$V_{LOW} = 10\text{V}, V_{HIGH} = 20\text{V}, R_1 = R_2 = 20 \text{ k}\Omega$
Sweep Range	1000:1	2000:1	2000:1	2000:1	2000:1		
Sweep Linearity							
10:1 Sweep	2	2	2	2	2		$f_H = f_L$
1000:1 Sweep	8	8	8	8	8		$f_H @ R_1 = 1 \text{ kHz}$
FM Distortion	0.1	0.1	0.1	0.1	0.1		$f_L @ R_1 = 2 \text{ M}\Omega$
Recommended Timing Components							
Timing Capacitor: C	0.001	100	0.001	100	100	µF	$f_L = 1 \text{ kHz}, f_H = 10 \text{ kHz}$
Timing Resistors: R_1 & R_2	1	2000	1	2000	2000	kΩ	$f_L = 100 \text{ Hz}, f_H = 100 \text{ kHz}$
Triangle/Sinewave Output							+10% Deviation
Triangle Amplitude							
Sinewave Amplitude							
Max. Output Swing	40	160	60	160	160	mV/KΩ	See Note 1, Fig. 3
Output Impedance	6	60	80	60	60	mV/KΩ	Fig. 2 S1 Open
Triangle Linearity	600	6	600	6	6	Vpp	Fig. 2 S1 Closed
Amp. Linearity	1	1	1	1	1	Ω	
Sinewave Amplitude Stability	0.5	0.5	0.5	0.5	0.5	%	For 1000:1 Sweep
	-4800	-4800	-4800	-4800	-4800	ppm/°C	See Note 2
Sinewave Distortion							D = 20 dB
Storage Temperature Range	-65°C to +150°C						
AVAILABLE TYPES							



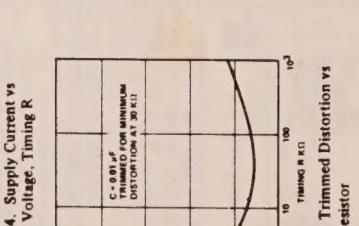
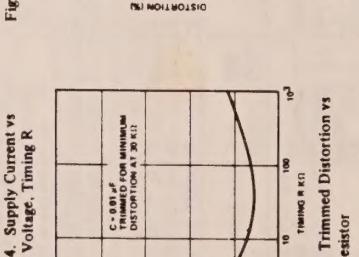
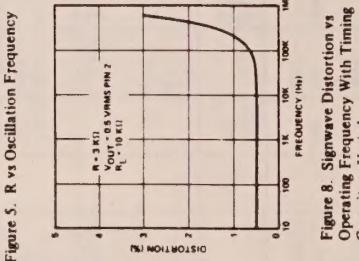
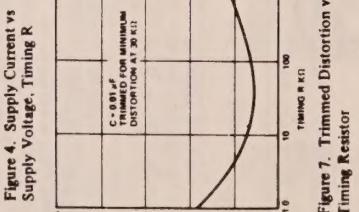
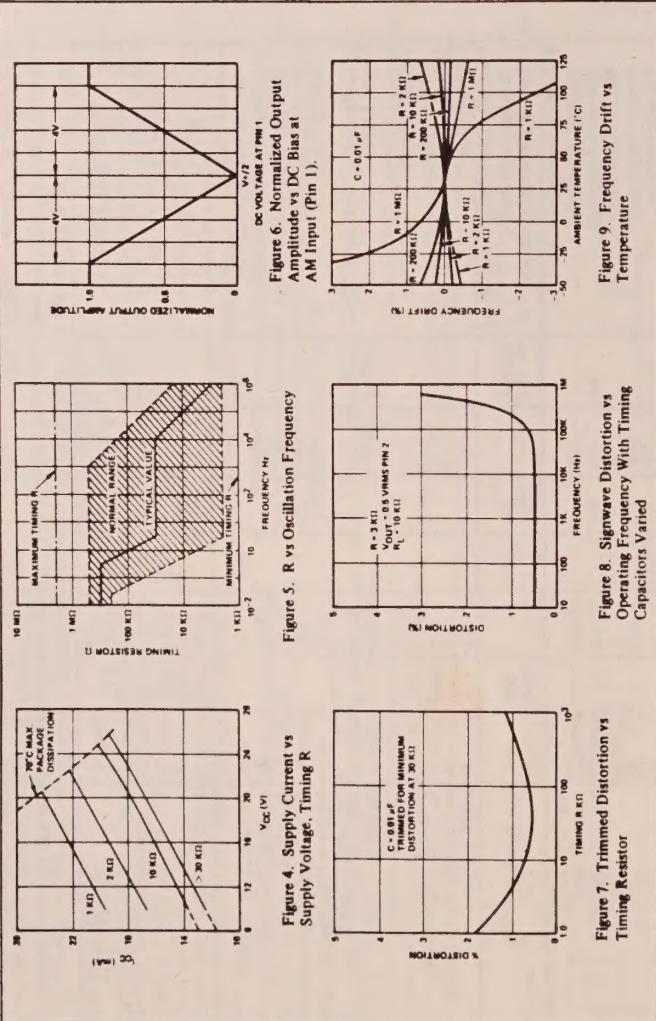
Note 1: Output amplitude is directly proportional to the resistance R_3 on pin 3. See figure 3. For maximum amplitude stability R_3 should be no more than 100 k Ω . **Note 2:** For higher output voltage, increase R_1 and decrease R_2 .



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1360 2. מלחין ועורך



DESCRIPTION OF CIRCUIT CONTROLS

FREQUENCY OF OPERATION:

The frequency of oscillation, f_0 , is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as

$$f_0 = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C . The recommended values of R for a given frequency range are shown in Figure 5. Temperature stability is optimum for $4 \text{ k}\Omega < R < 200 \text{ k}\Omega$. Recommended values of C are from 1000 pF to $100 \mu\text{F}$.

FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is proportional to the total timing current I_T drawn from pin 7 or 8

$$f = \frac{320I_T(\text{mA})}{C(\mu\text{F})} \text{ Hz}$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at $+3\text{V}$, with respect to pin 12. Frequency varies linearly with I_T over a wide range of current values, from $1 \mu\text{A}$ to 3 mA . The frequency can be controlled by applying a control voltage, V_C , to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC} \left[1 + \frac{R}{RC} \left(1 - \frac{V_C}{3} \right) \right] \text{ Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K , is given as:

$$K = \frac{\partial I / \partial V_C}{R_C} = -\frac{0.32}{R_C C} \text{ Hz/V}$$

NOTE: For safe operation of the circuit pins 7 and 8, respectively, as shown in Figure 13, depending on the polarity of the logic signal at pin 9, either one or the other of these timing

resistors is activated. If pin 9 is open-circuited or connected to a bias voltage $\geq 2\text{V}$, only R_1 is active. Similarly, if the voltage level at pin 9 is $\leq 1\text{V}$, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2 as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at pin 9 is referenced to V^- .

OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In Figures 11, 12 and 13, pin 3 is biased mid-way between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

SINEWAVE GENERATION

A) Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer R_1 at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the typical distortion (THD) is $< 2.5\%$. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with V^- . For split supply operation, R_3 can be directly connected to ground.

B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to $\approx 0.5\%$ by additional adjustments as shown in Figure 12. The potentiometer R_A adjusts the sine-shaping resistor; and can be adjusted by a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately $100 \text{ k}\Omega$. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ± 4 volts of $V^+/2$ as shown in Fig. 6. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB .

Amplitude Modulation: Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately $100 \text{ k}\Omega$. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ± 4 volts of $V^+/2$ as shown in Fig. 6. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB .

Note: AM control must be used in conjunction with a well-regulated supply since the output amplitude now becomes a function of V^+ .

FREQUENCY-SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2 , connected to the timing pins 7 and 8, respectively, as shown in Figure 13. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing

and R_B provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

- Set R_B at mid-point and adjust R_A for minimum distortion.
- With R_A set as above, adjust R_B to further reduce distortion.

TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sinewave output.

FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors R_1 and R_2 ; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^- .

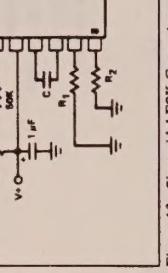


Figure 13. Sinusoidal FSK Generator

PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2 . The values of R_1 and R_2 should be in the range of $1 \text{ k}\Omega$ to $2 \text{ M}\Omega$.

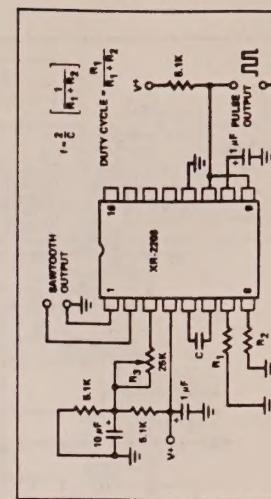


Figure 14. Circuit for Pulse and Ramp Generation